

FIG. 1

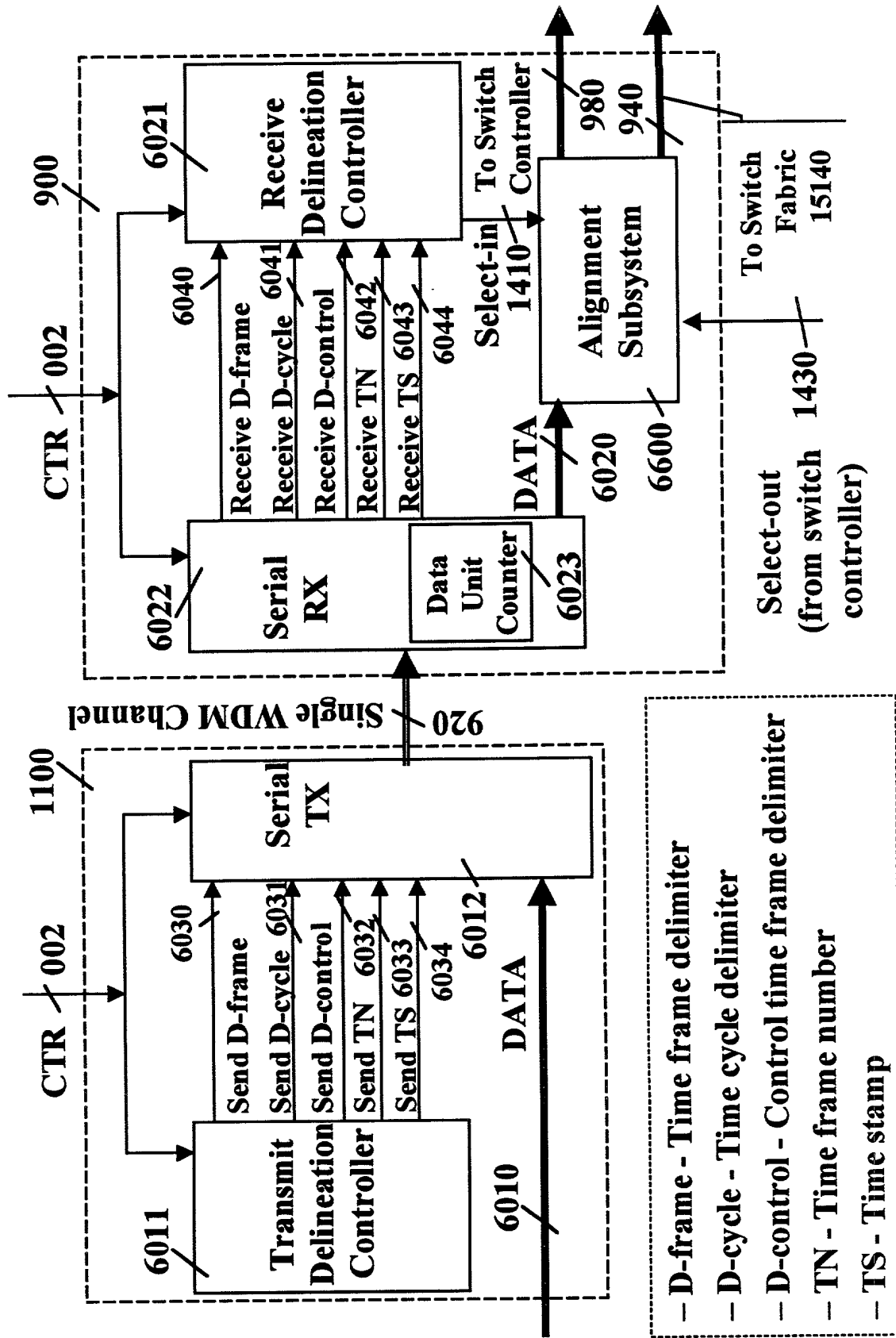


FIG. 2

Example:

TF1=15.325 microsec - High_capacity = OC-192

TF2 = 125 microsec - Low_capacity = OC-3

$\Rightarrow c = 64 = (OC-192/OC-3)$

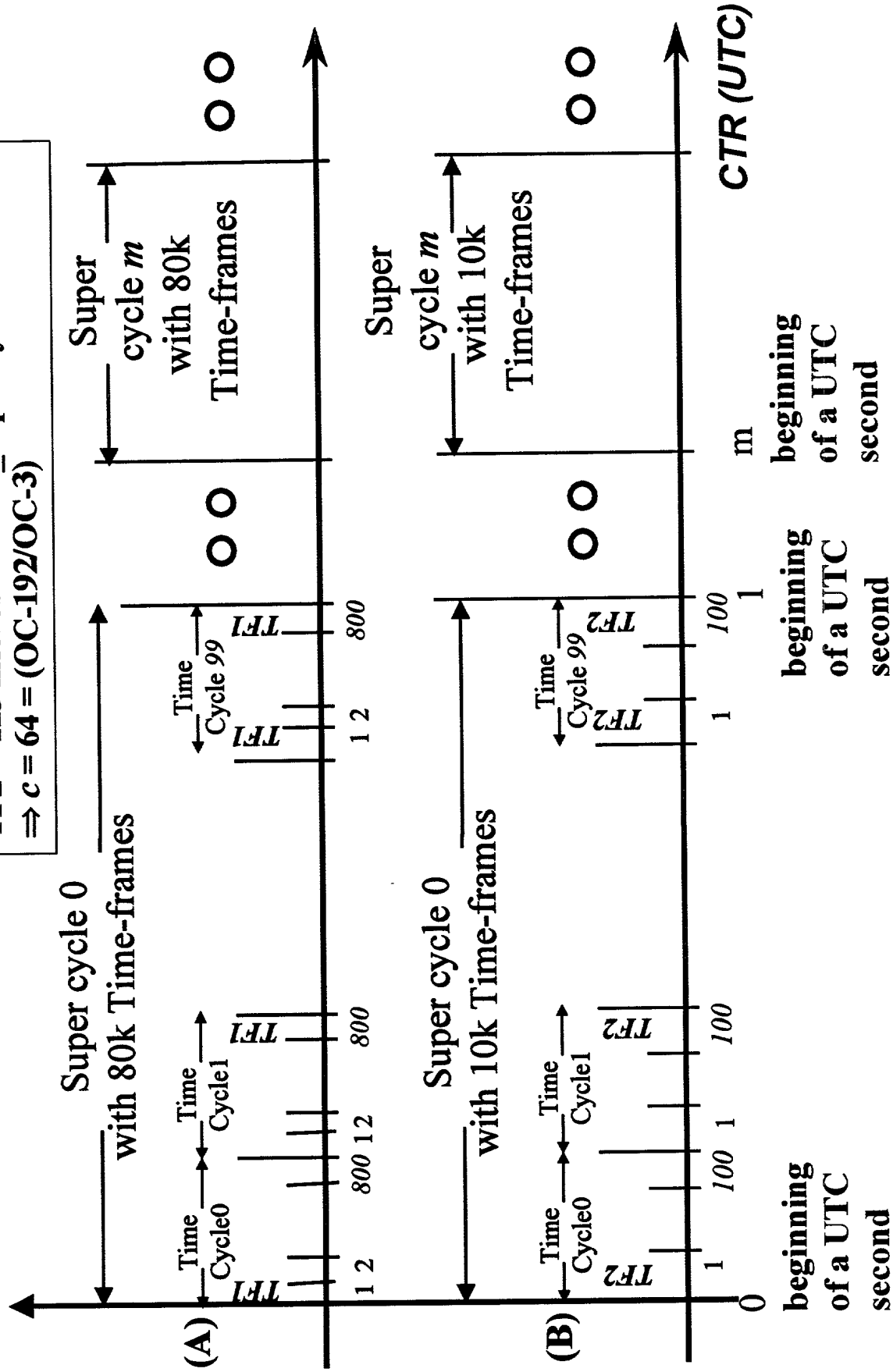


FIG. 3

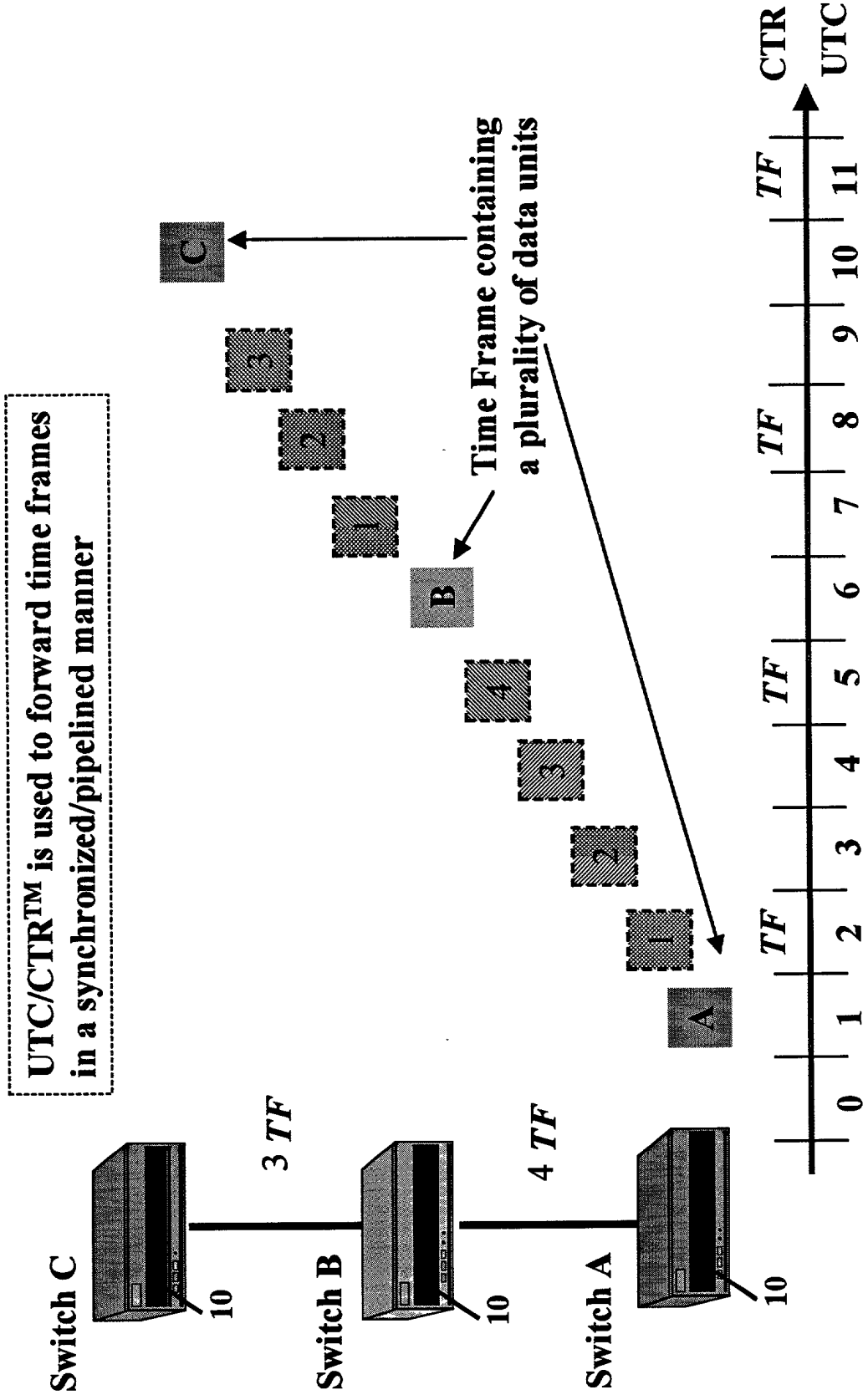
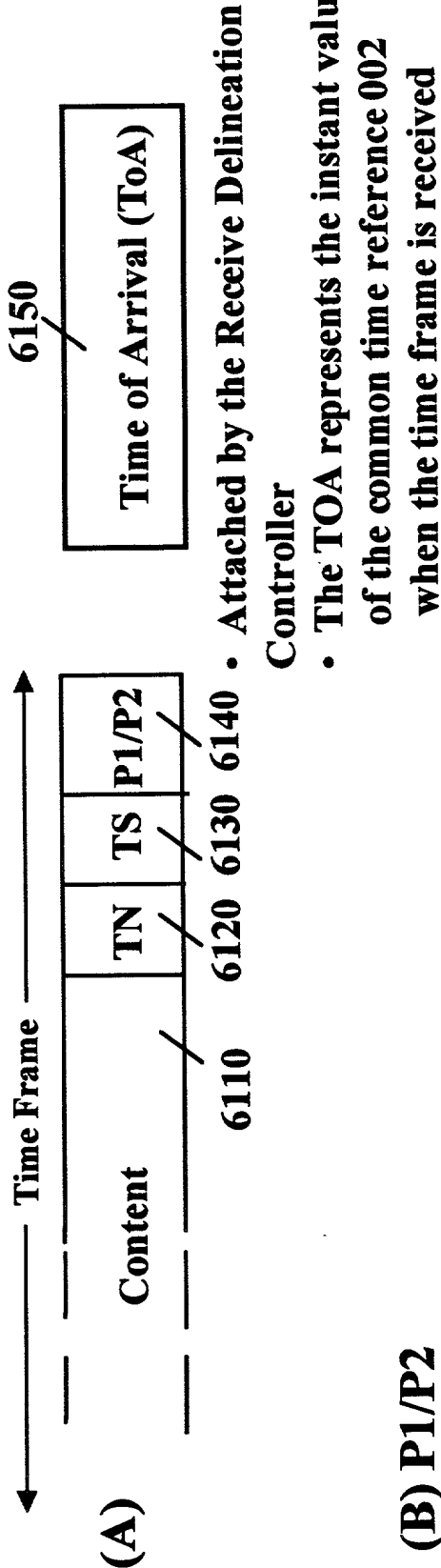


FIG. 4



(B) P1/P2

- P1/P2=00 D-frame - Time frame delimiter
- P1/P2=01 D-cycle - Time cycle delimiter
- P1/P2=10 D-control - Control time frame delimiter

TN - Time frame number
TS - Time stamp

FIG. 5

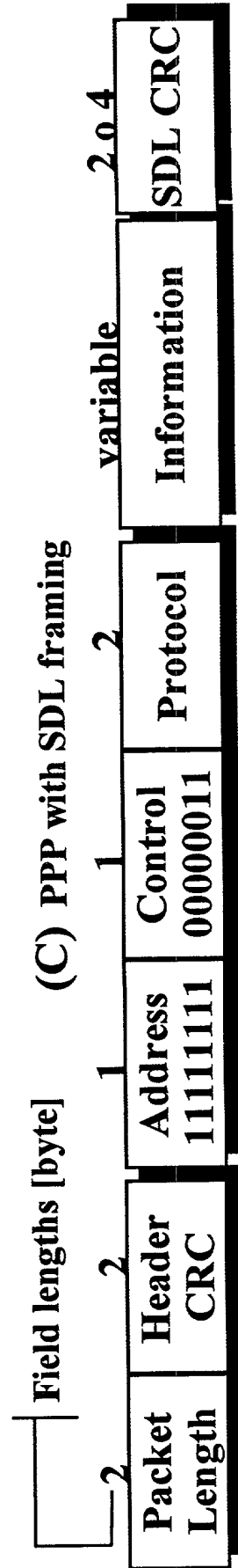
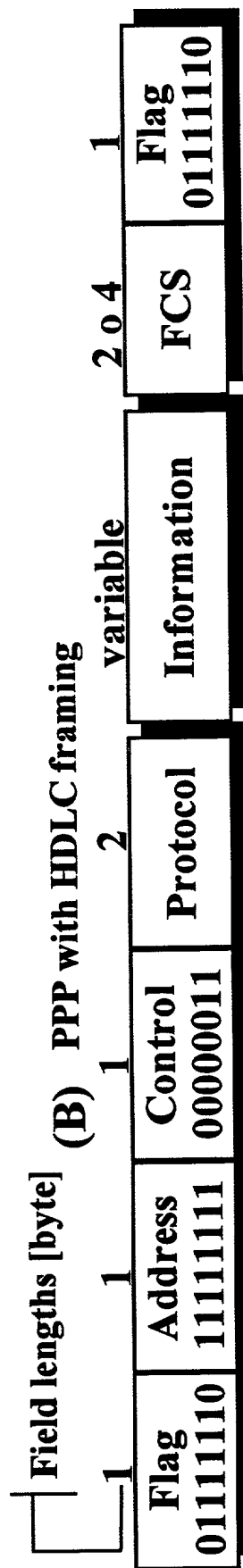
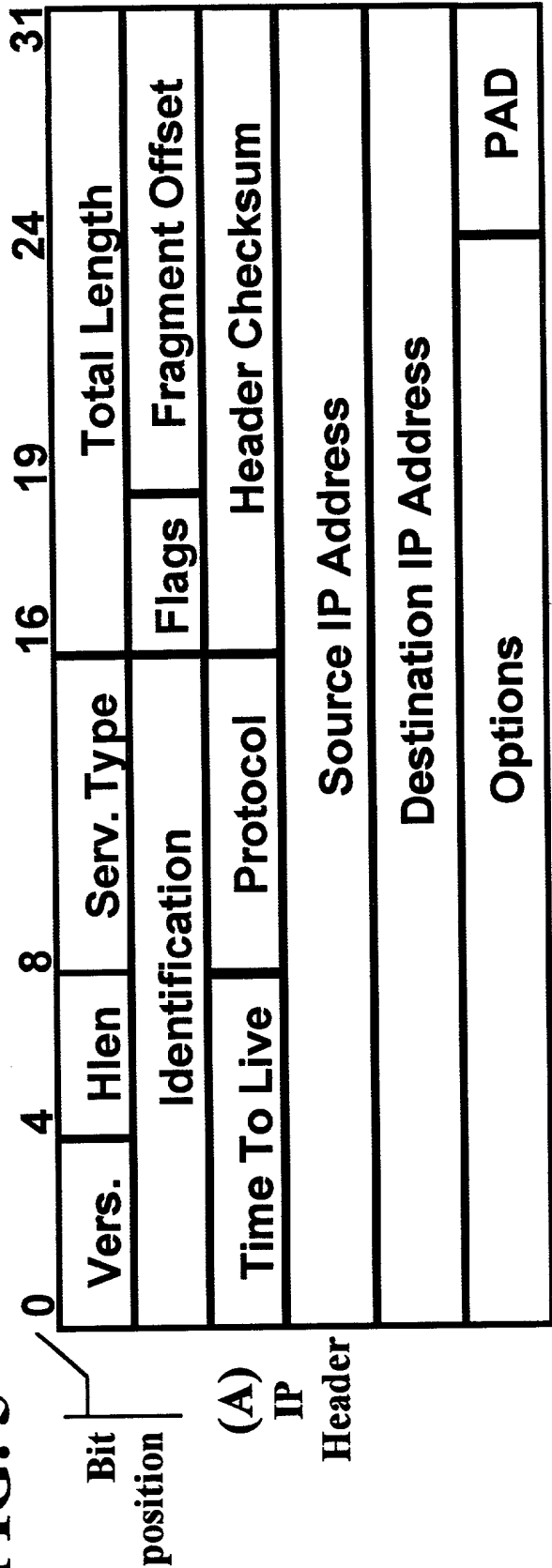


FIG. 6

- SONET - synchronous optical network
- Multiplexing method: byte interleaving
- Signal hierarchy: OC-N (STS-N)
 - STS-N rate: $N \times 51.84$ Mb/s
 - Frame format: 9 rows by $90 \times N$ columns
 - capacity: $N \times 810$ bytes in 125 microsecond.
 - overhead: $N \times 27$ bytes
 - payload: $N \times 783$ bytes

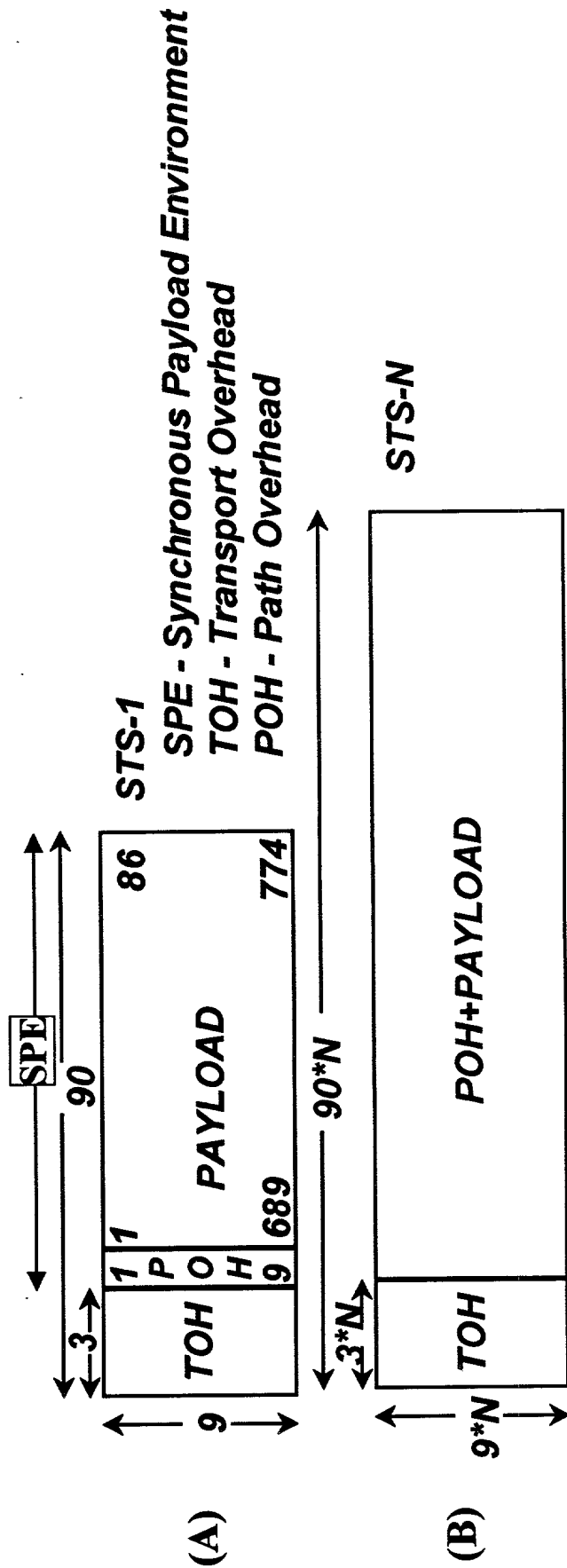
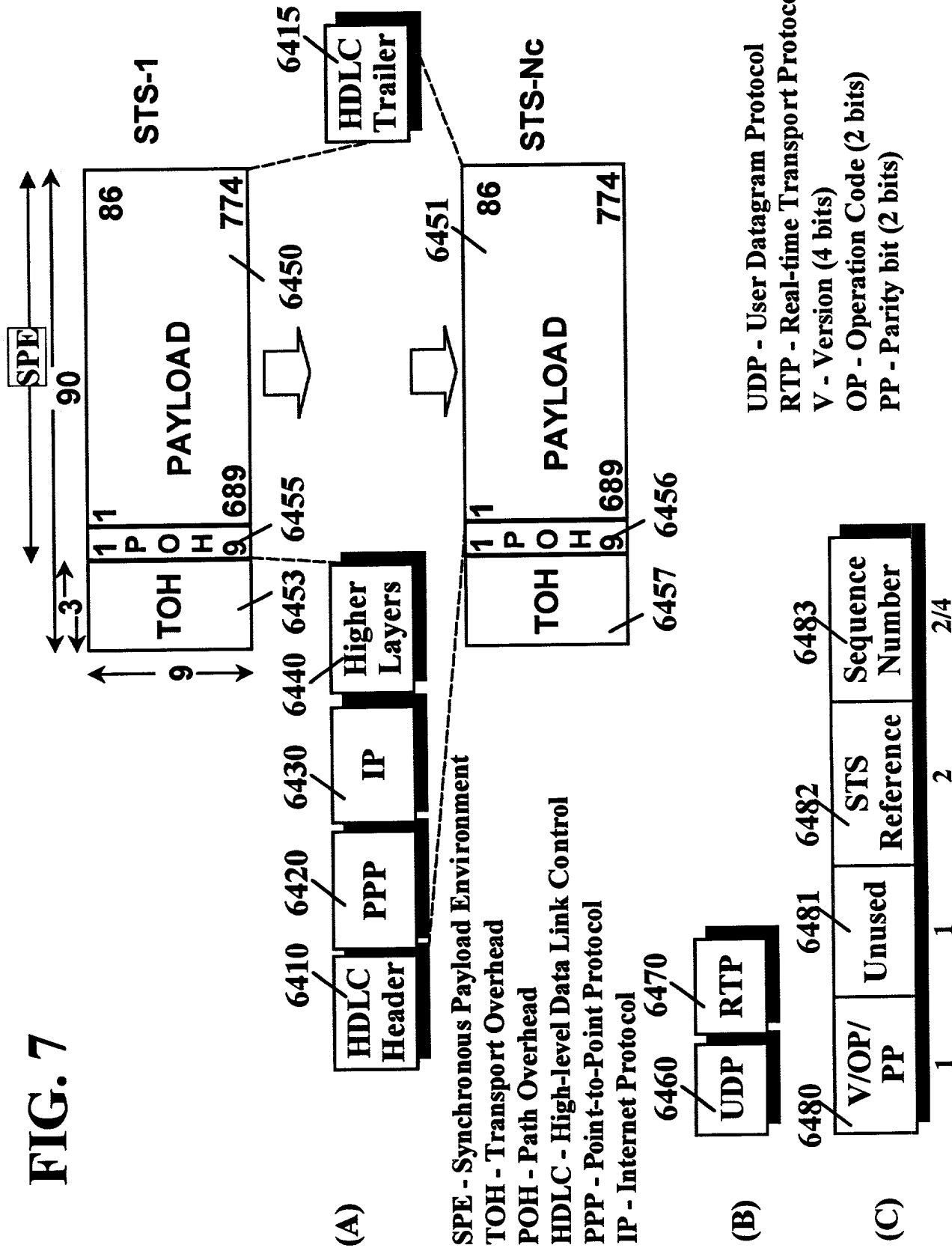
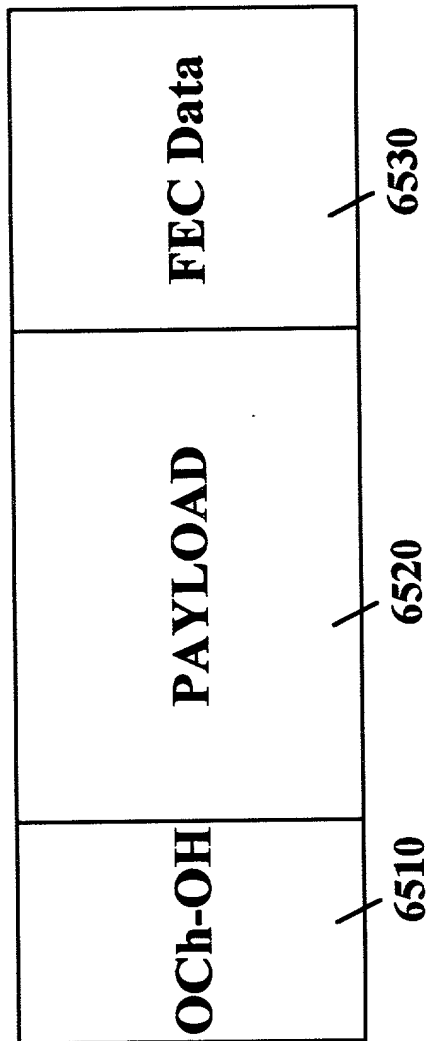


FIG. 7



UDP - User Datagram Protocol
RTP - Real-time Transport Protocol
V - Version (4 bits)
OP - Operation Code (2 bits)
PP - Parity bit (2 bits)

FIG. 8



OCh - Optical Channel
OH - Overhead
FEC - Forward Error Correction

FIG. 9

TF Alignment of UTR(i) to UTC - with three input queues - principle of operation:

The same queue is not used simultaneously for:

1. Receiving data packets from the serial link, and
2. Forwarding data packets to the switch fabric

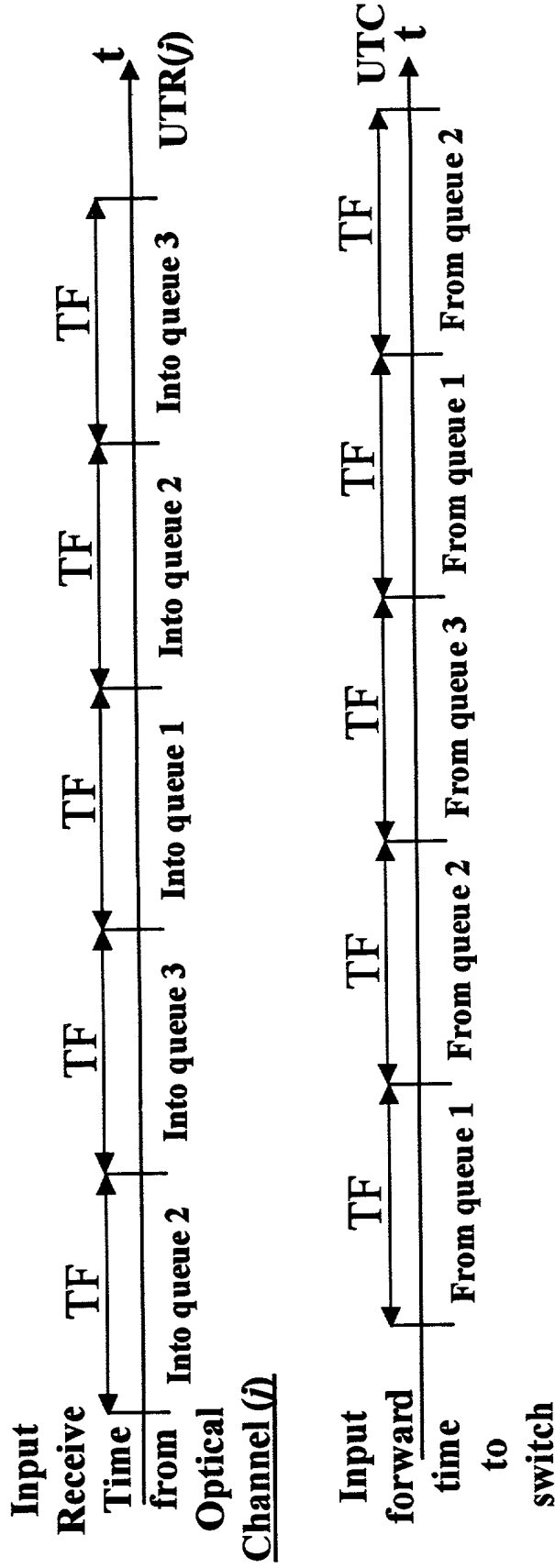
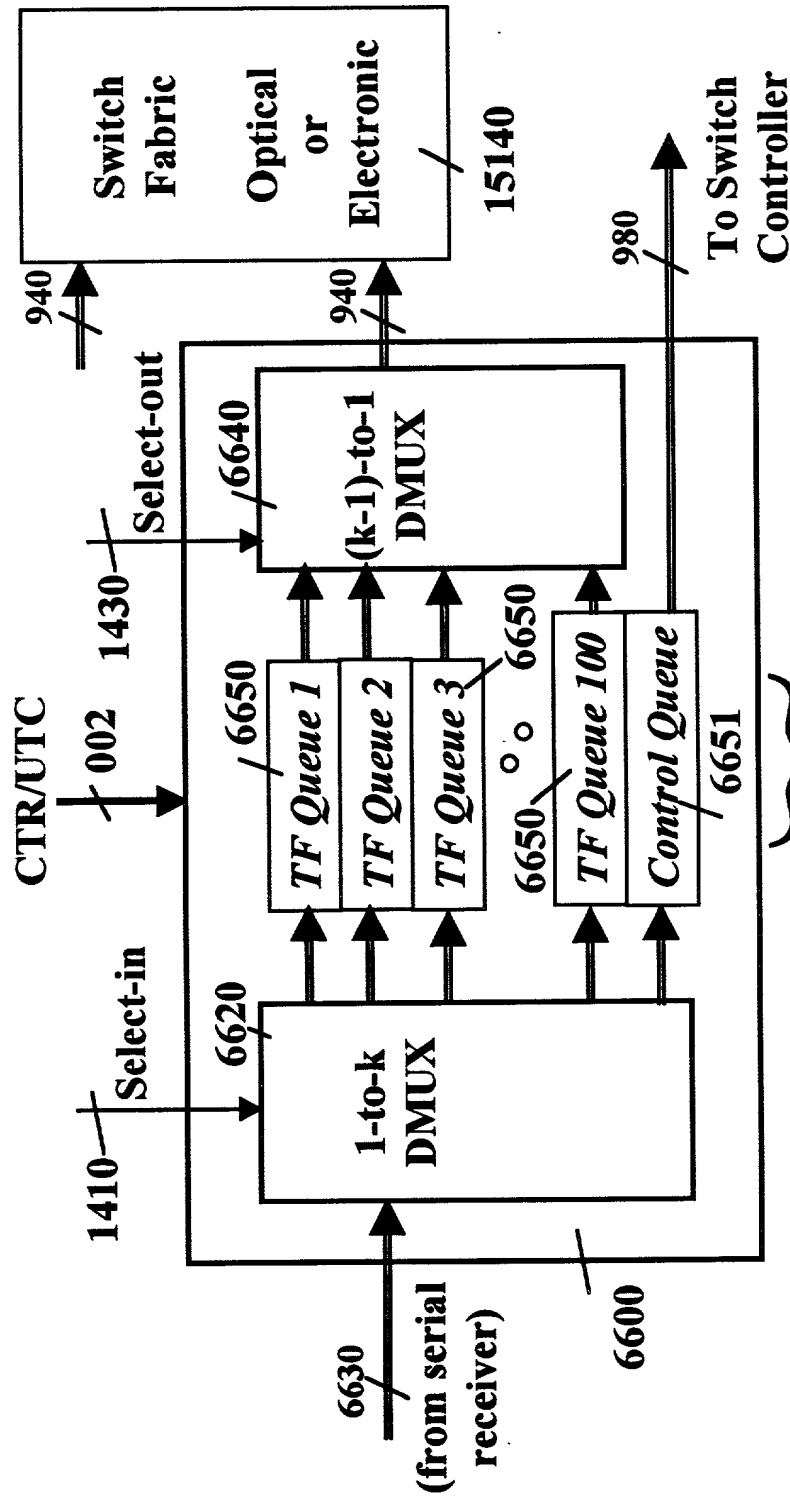


FIG. 10



Alignment Subsystem for Channel j at Input Port i
 with a Plurality of k Time Frame Queues, where k is
 the number of time frames in one time cycle

FIG. 11

Maximum alignment subsystem requirements for
local recovery from arbitrary timing failure:
- For immediate recovery a time measurement time stamp
should be sent every time frame and/or time cycle.

Time Cycle	OC-48 – 2.4 Gb/s	OC-192 – 9.6 Gb/s
1 ms	0.3 MByte	1.2 MByte
2 ms	0.6 MByte	2.4 MByte
4 ms	1.2 MByte	4.8 MByte
10 ms	3 MByte	12 MByte
20 ms	6MByte	24 MByte

FIG. 12

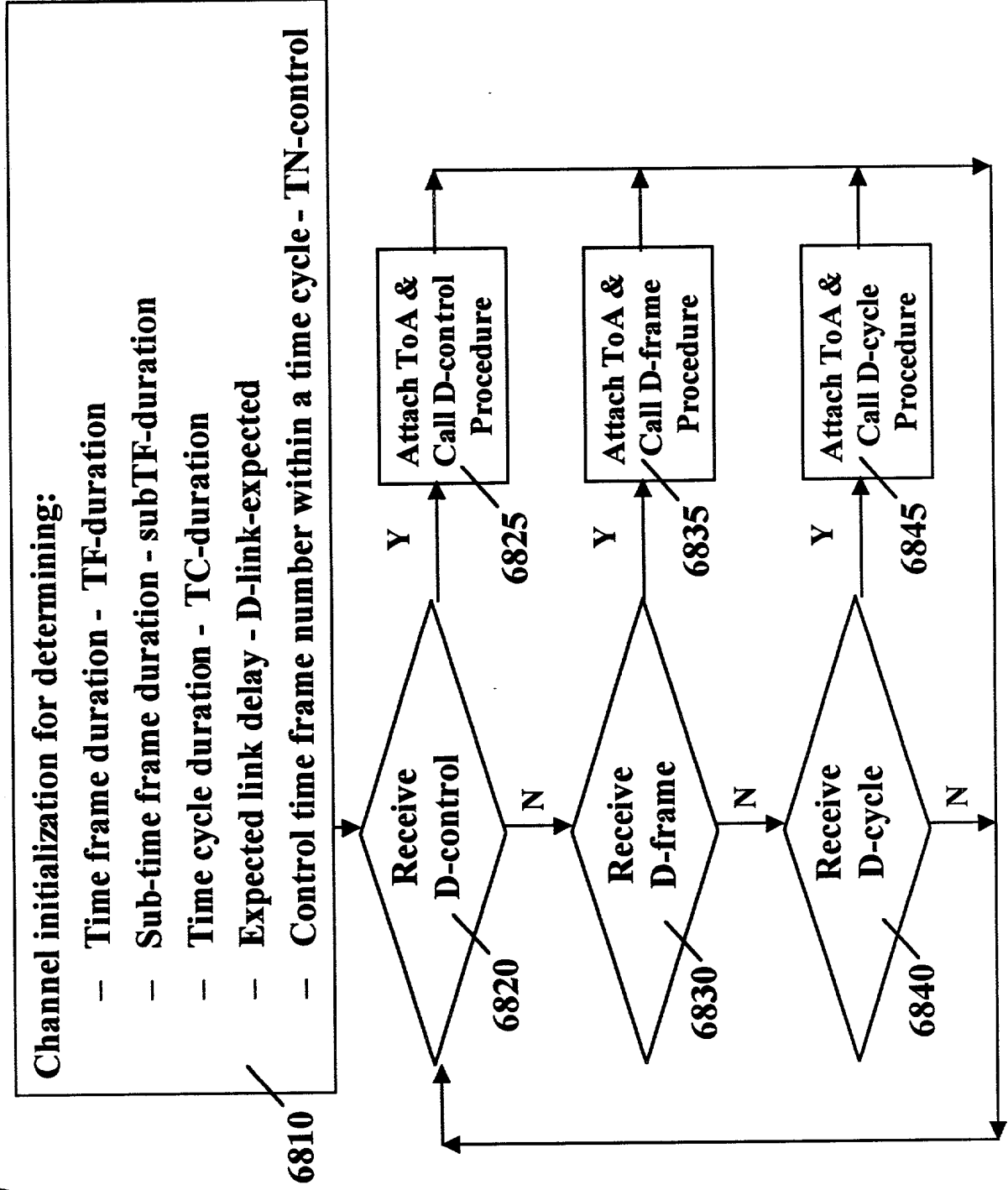


FIG. 13

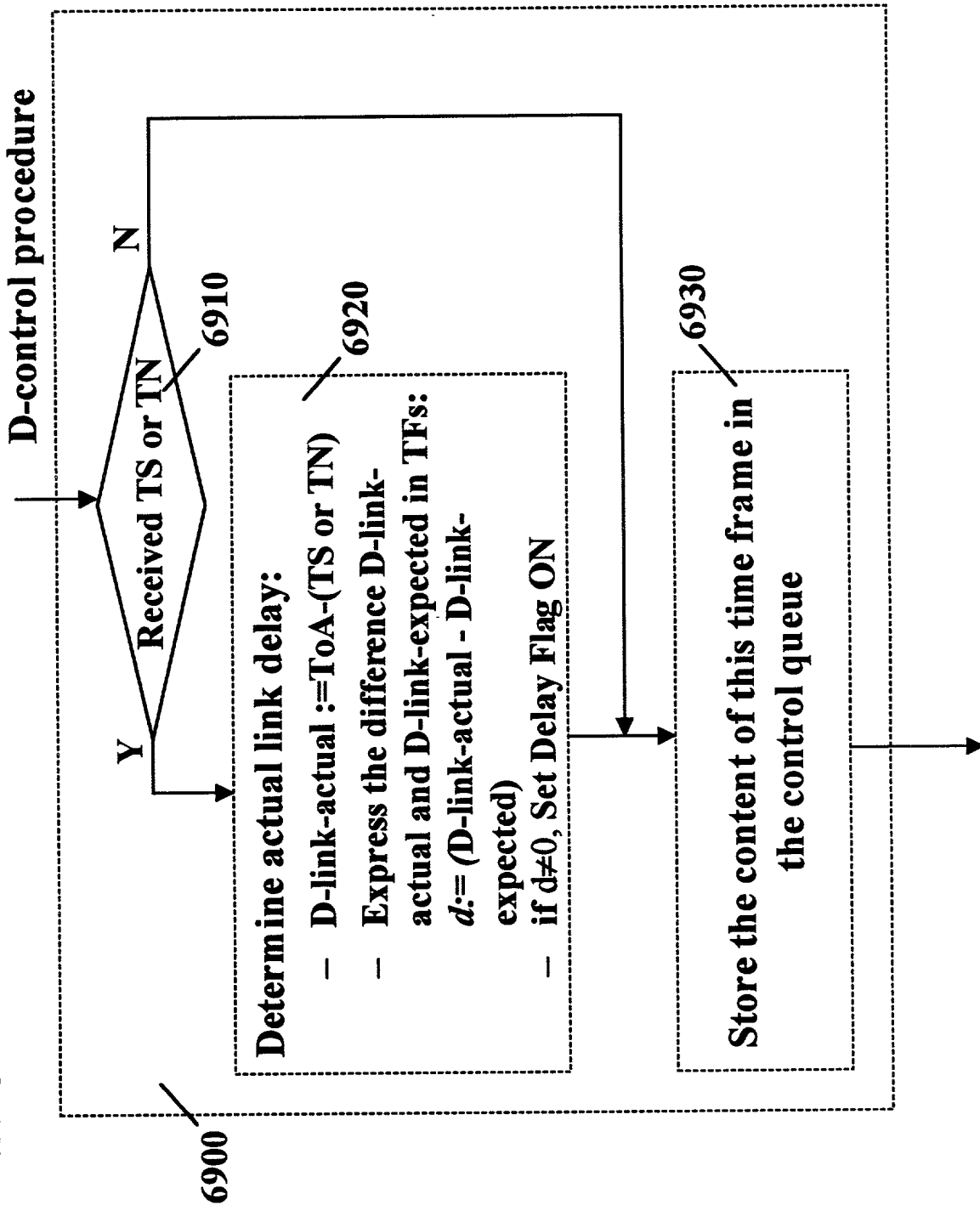


FIG. 14

D-frame procedure

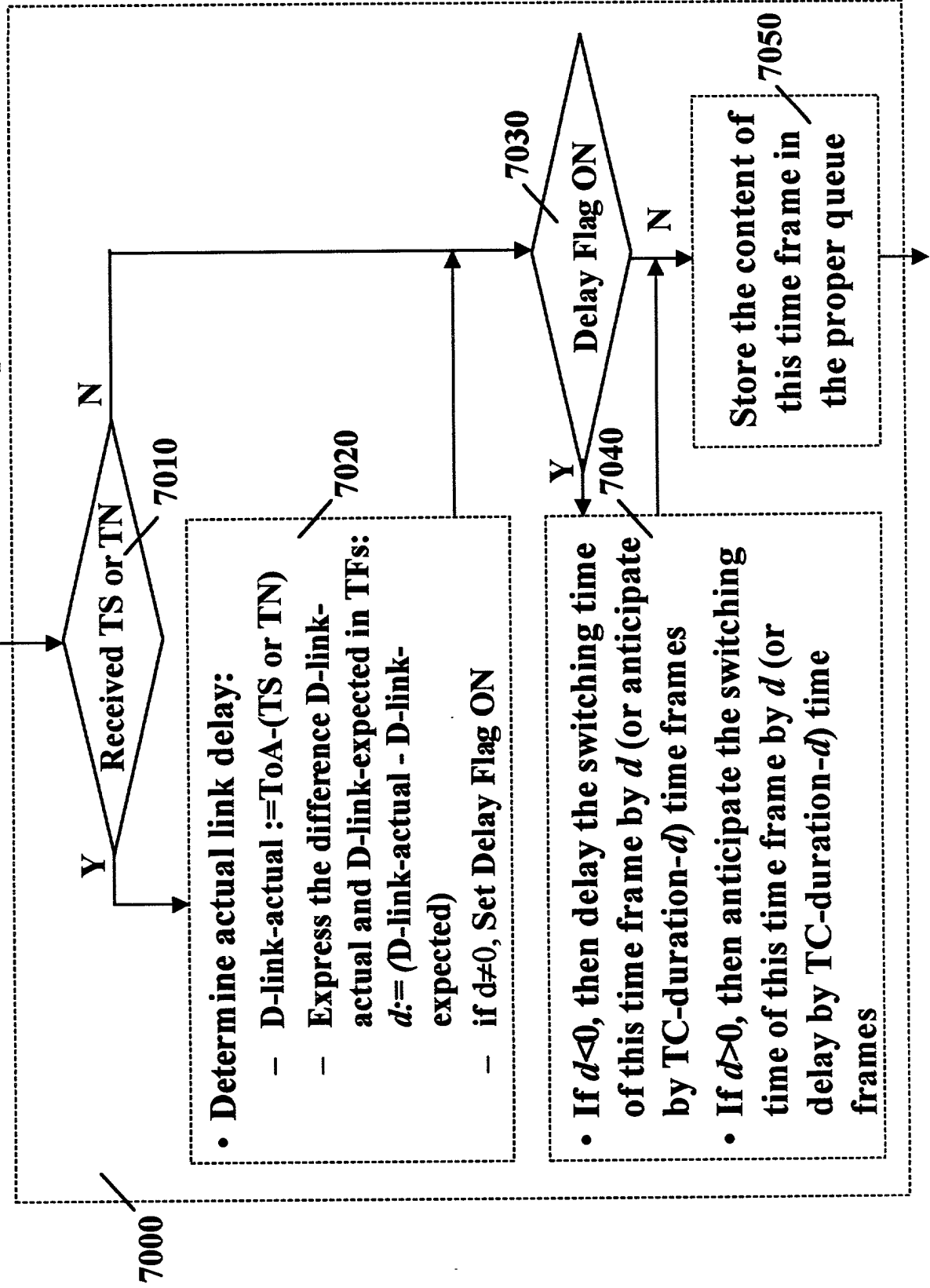
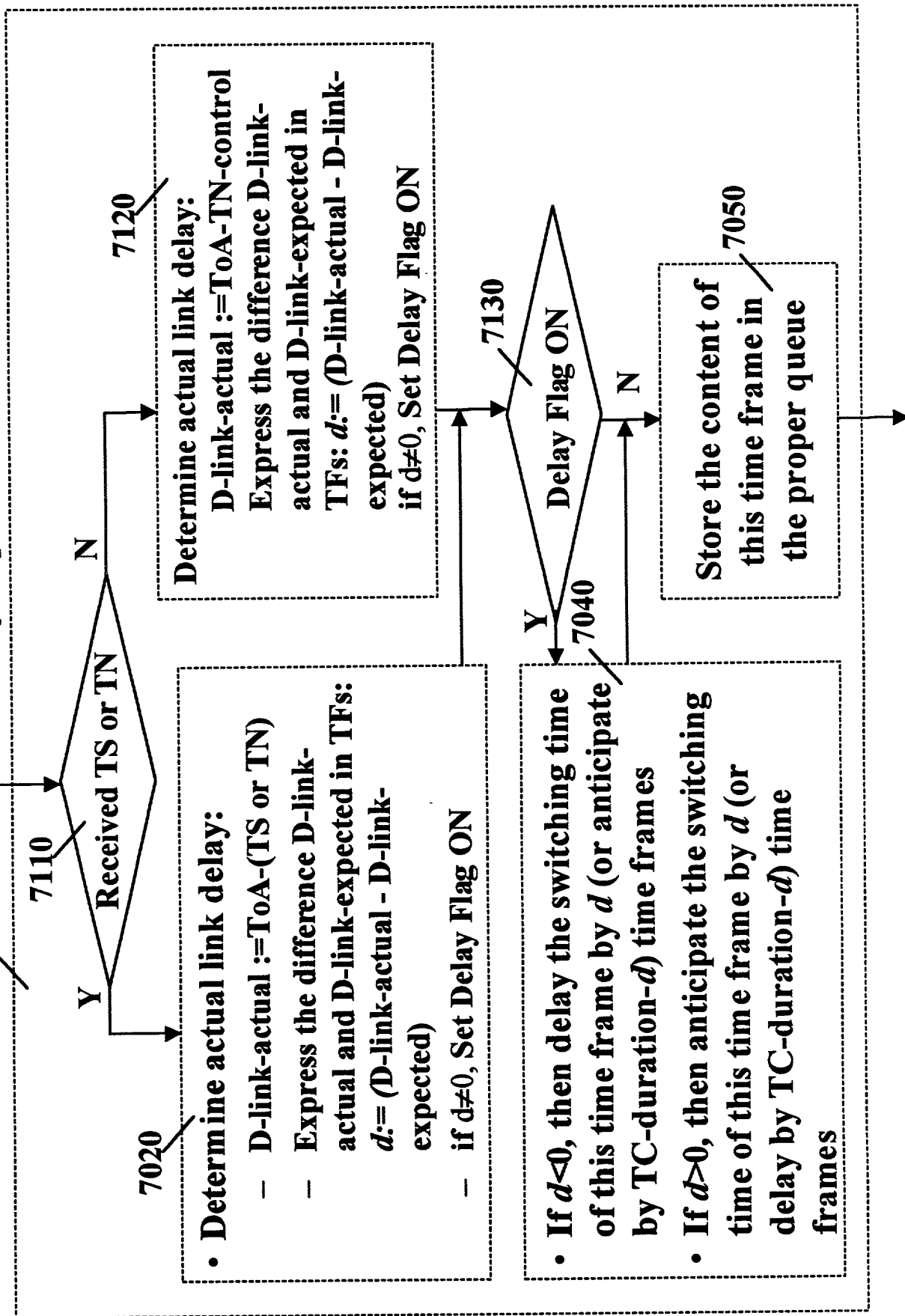


FIG. 15

D-cycle procedure



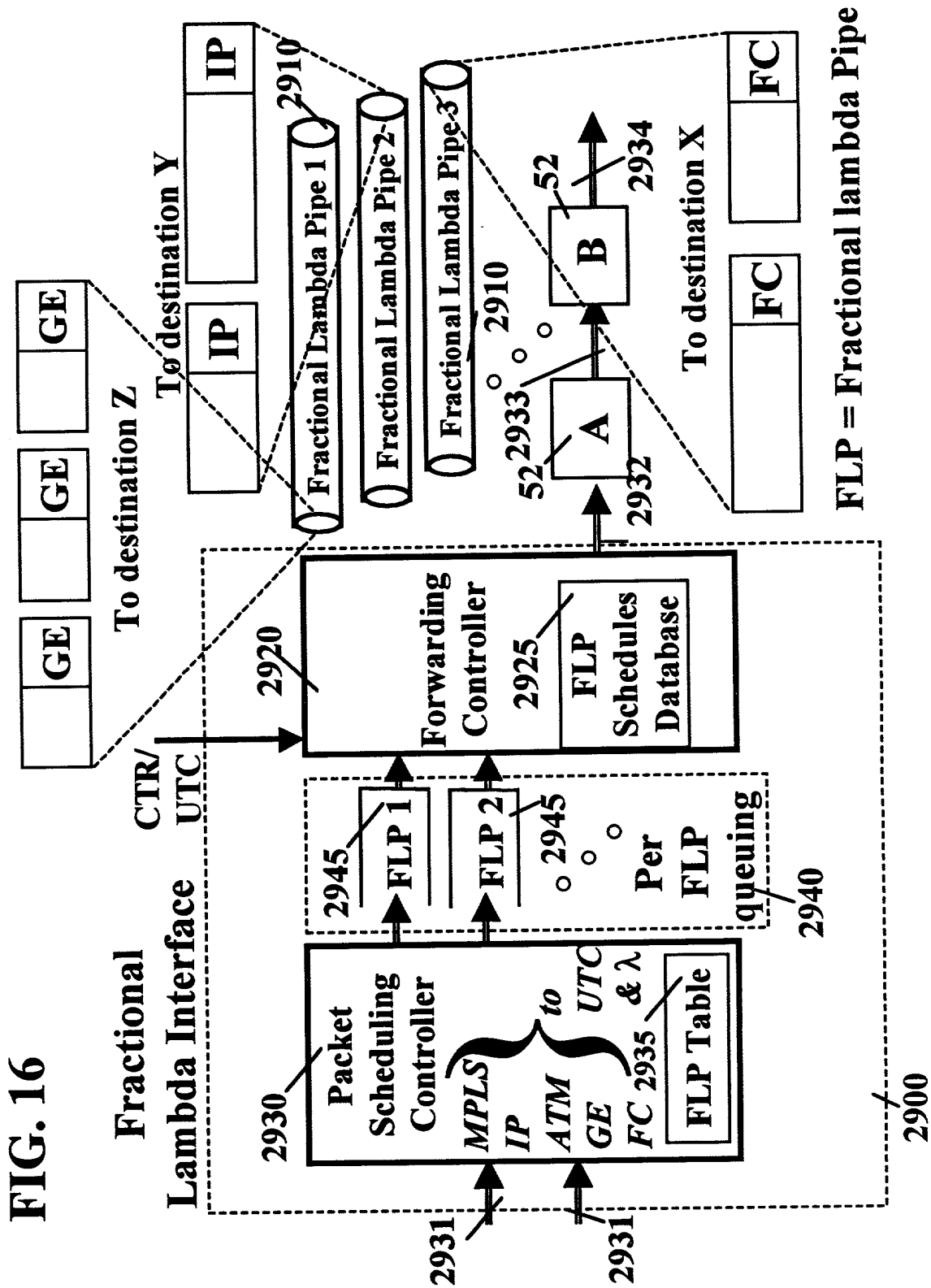


FIG. 17

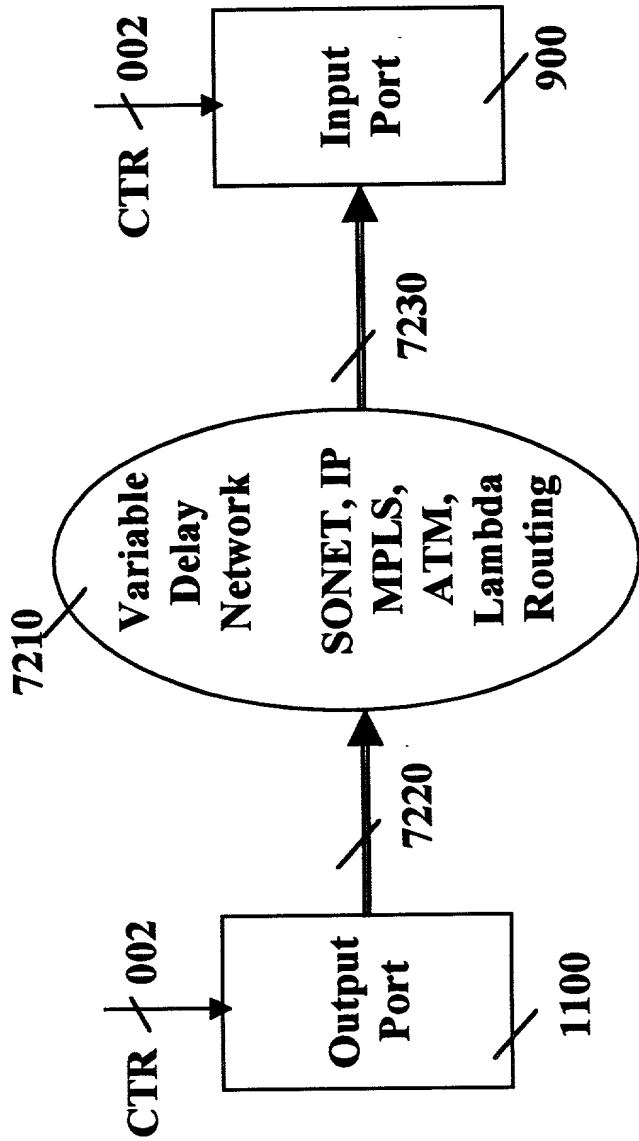


FIG. 18

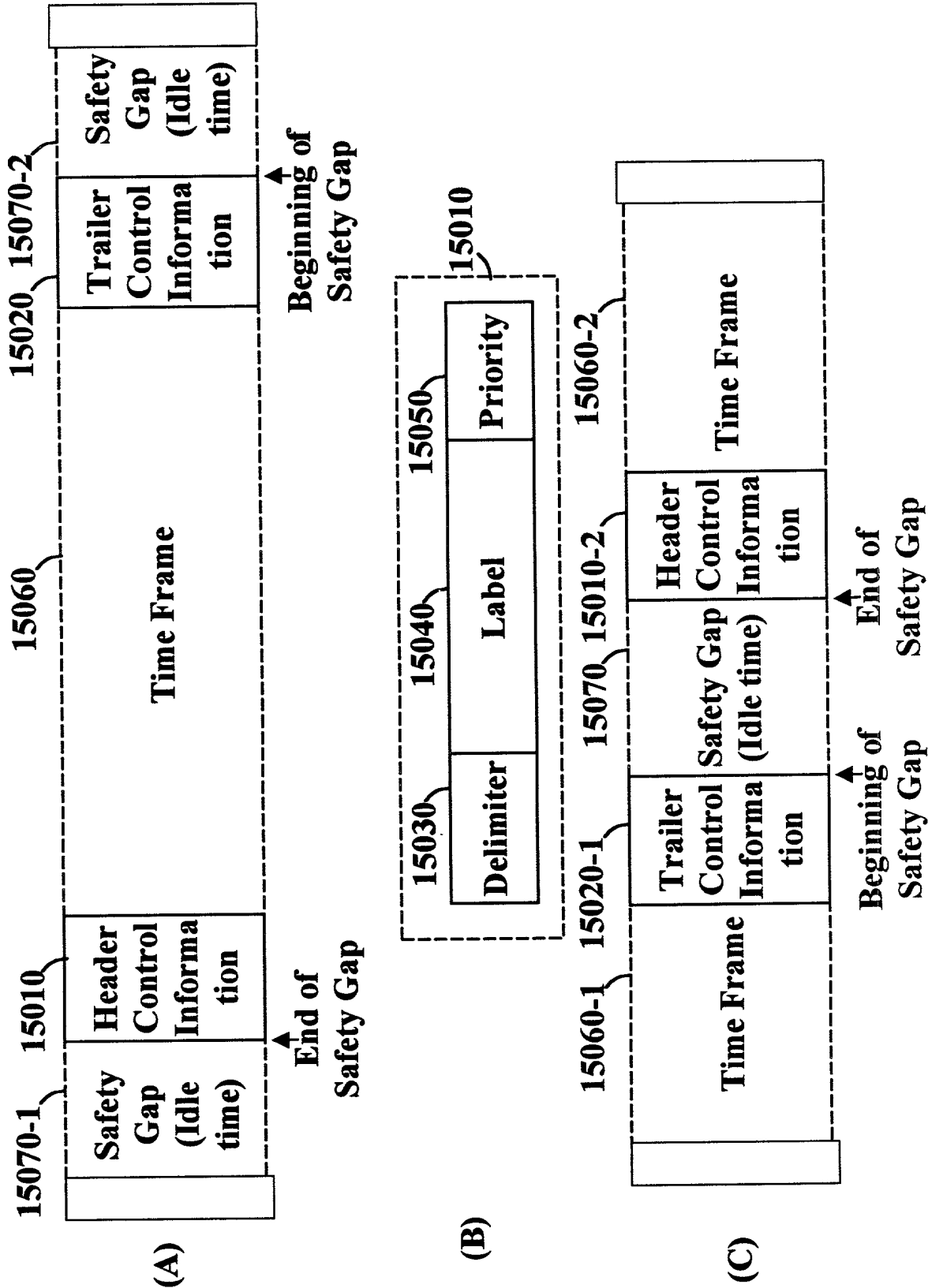


FIG. 19

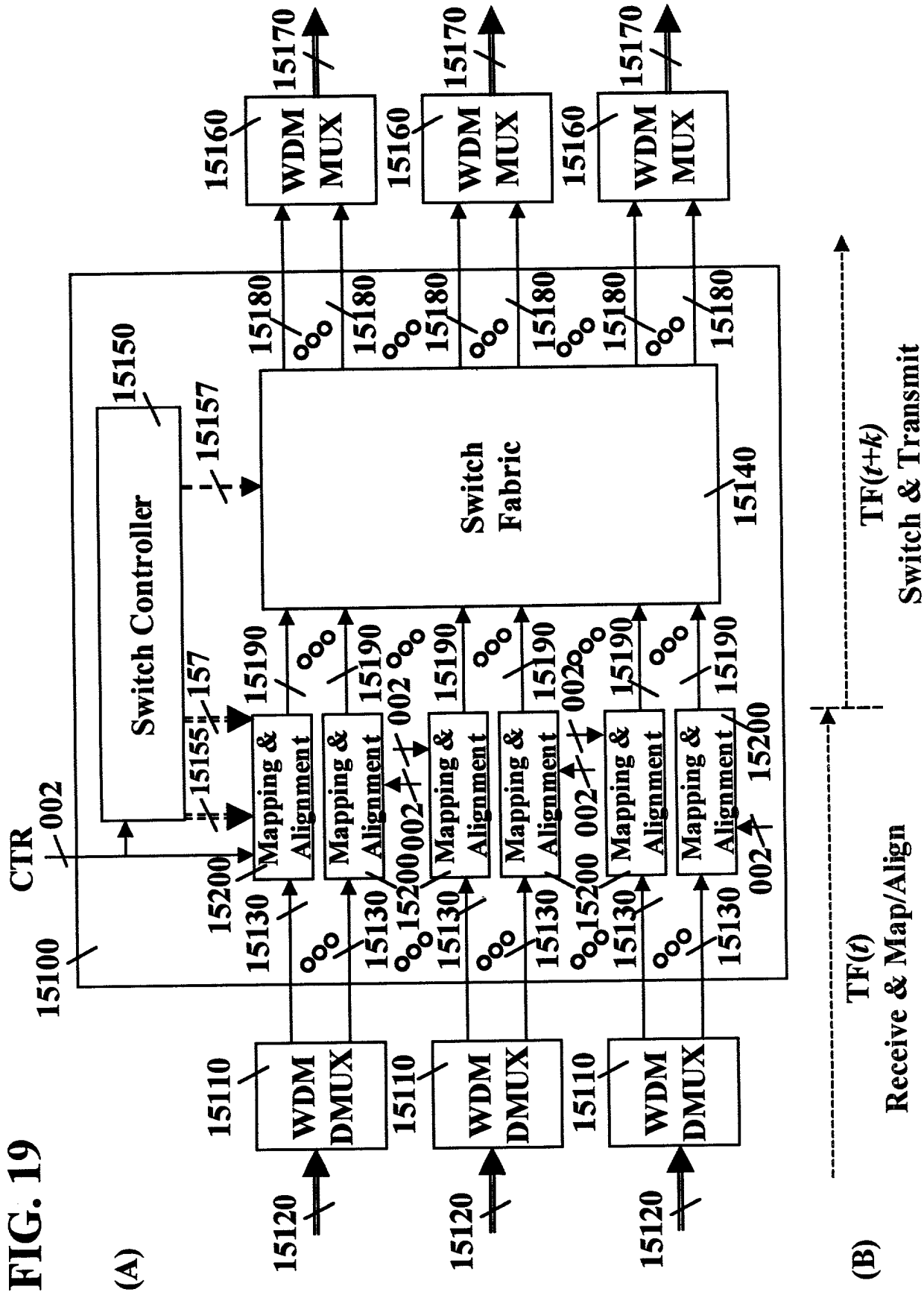


FIG. 20

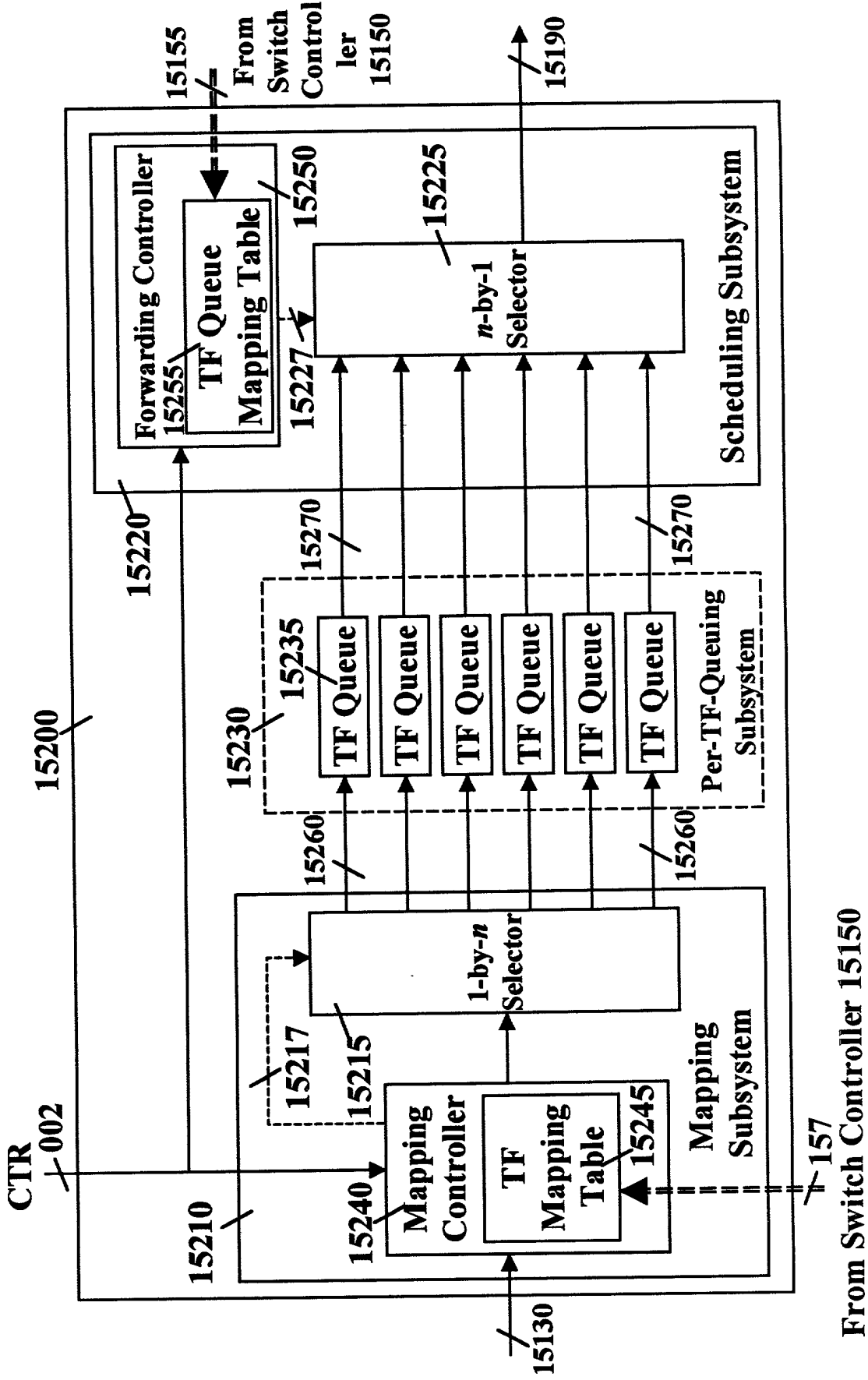


FIG. 21

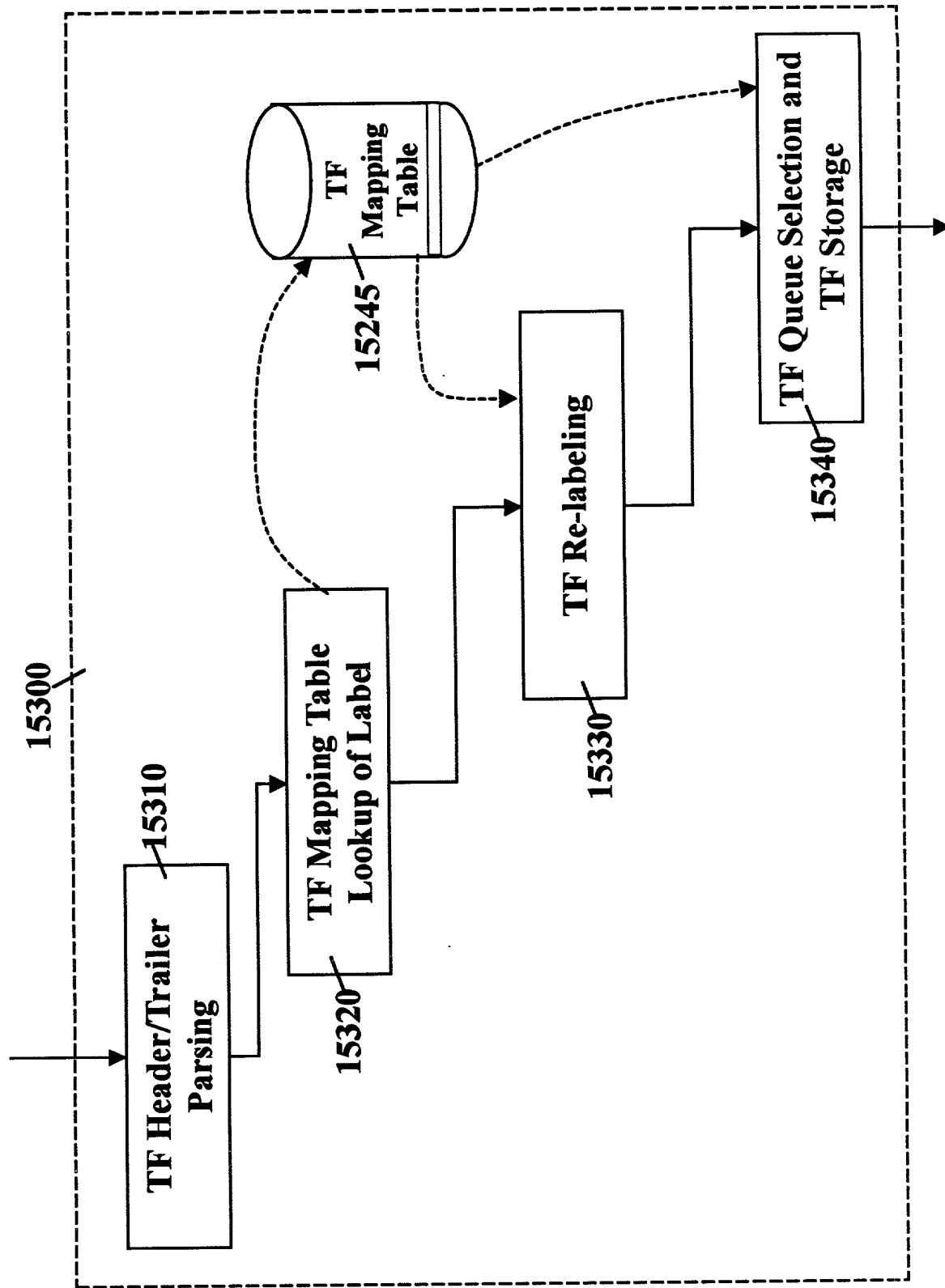


FIG. 22

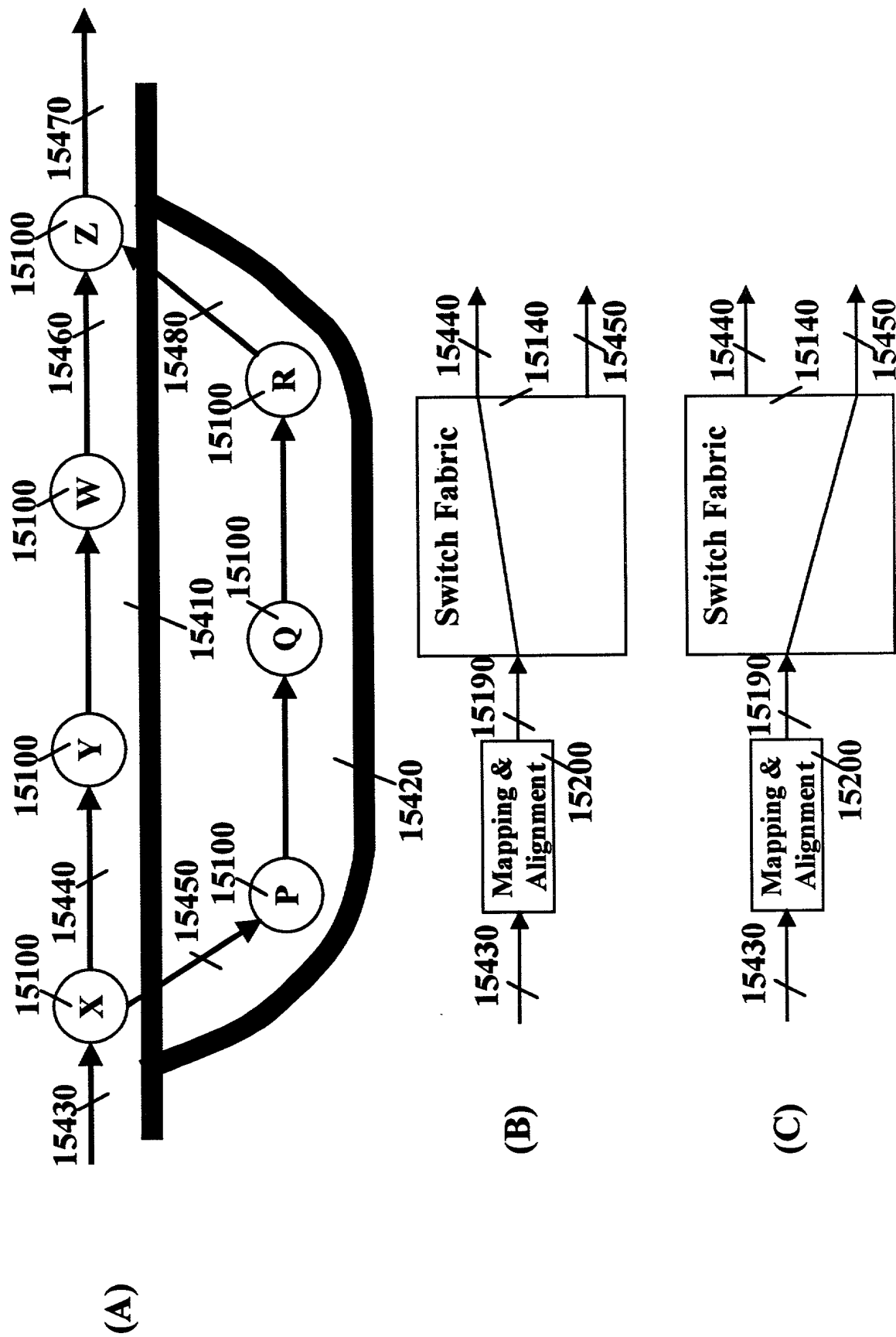


FIG. 23

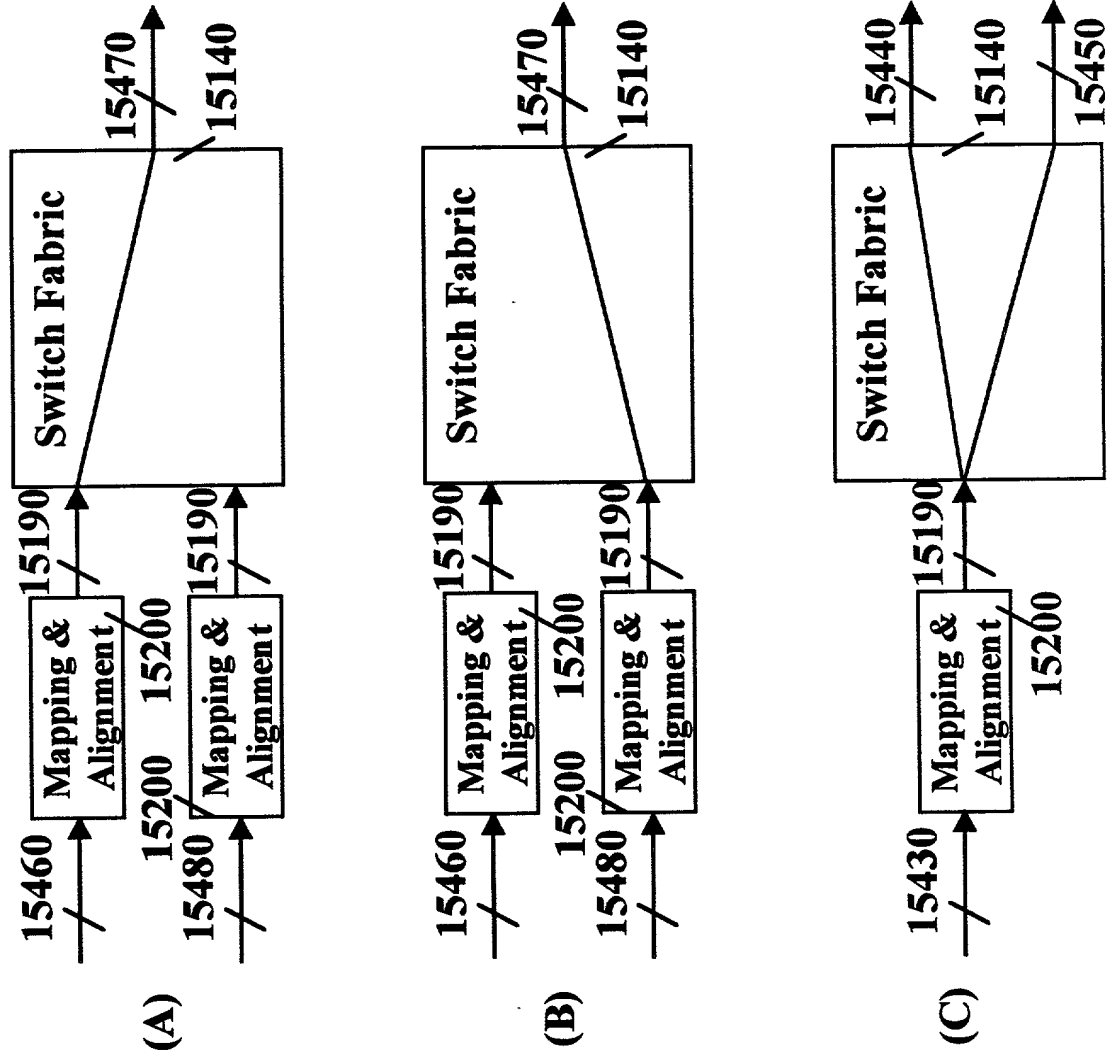


FIG. 24

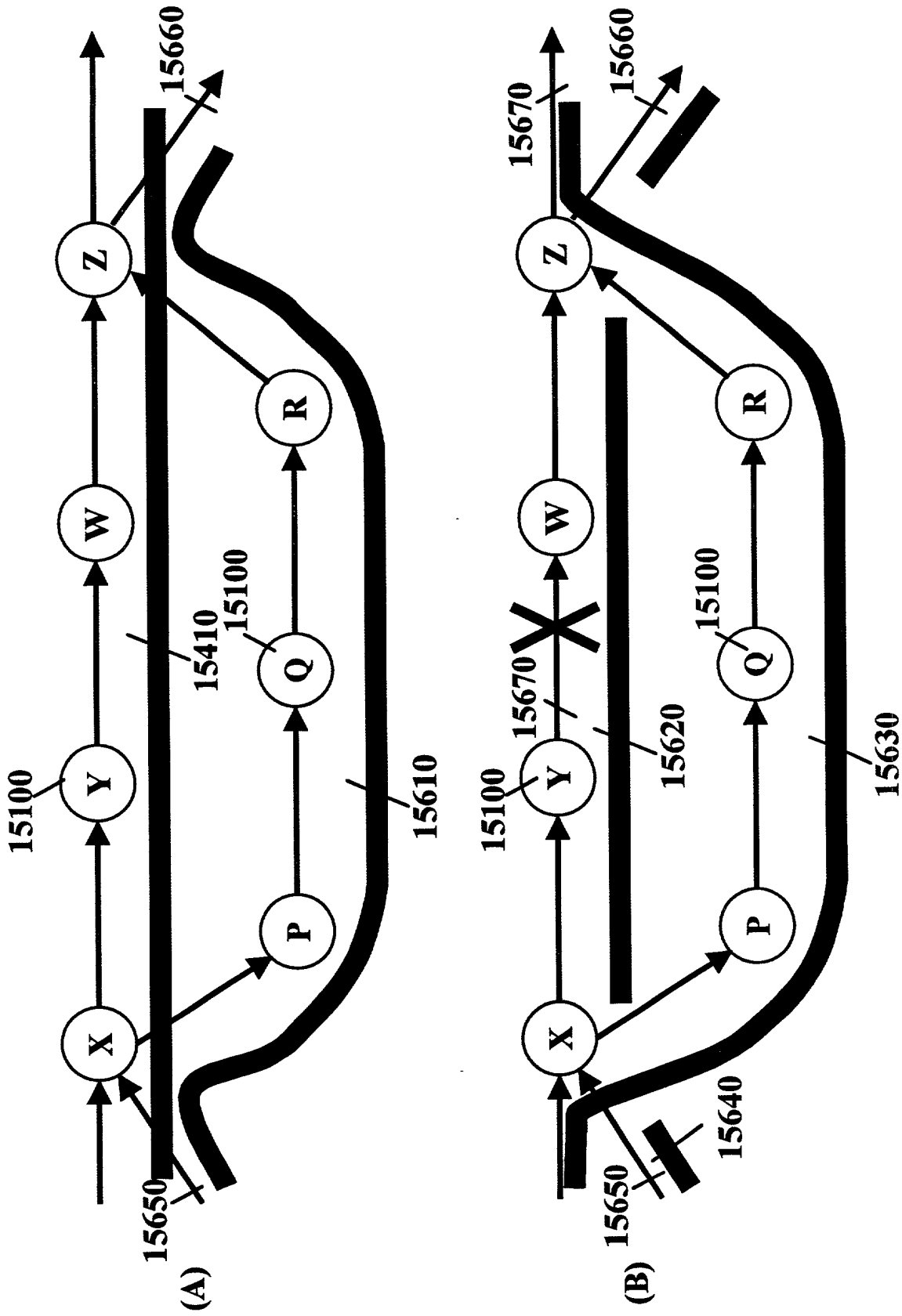
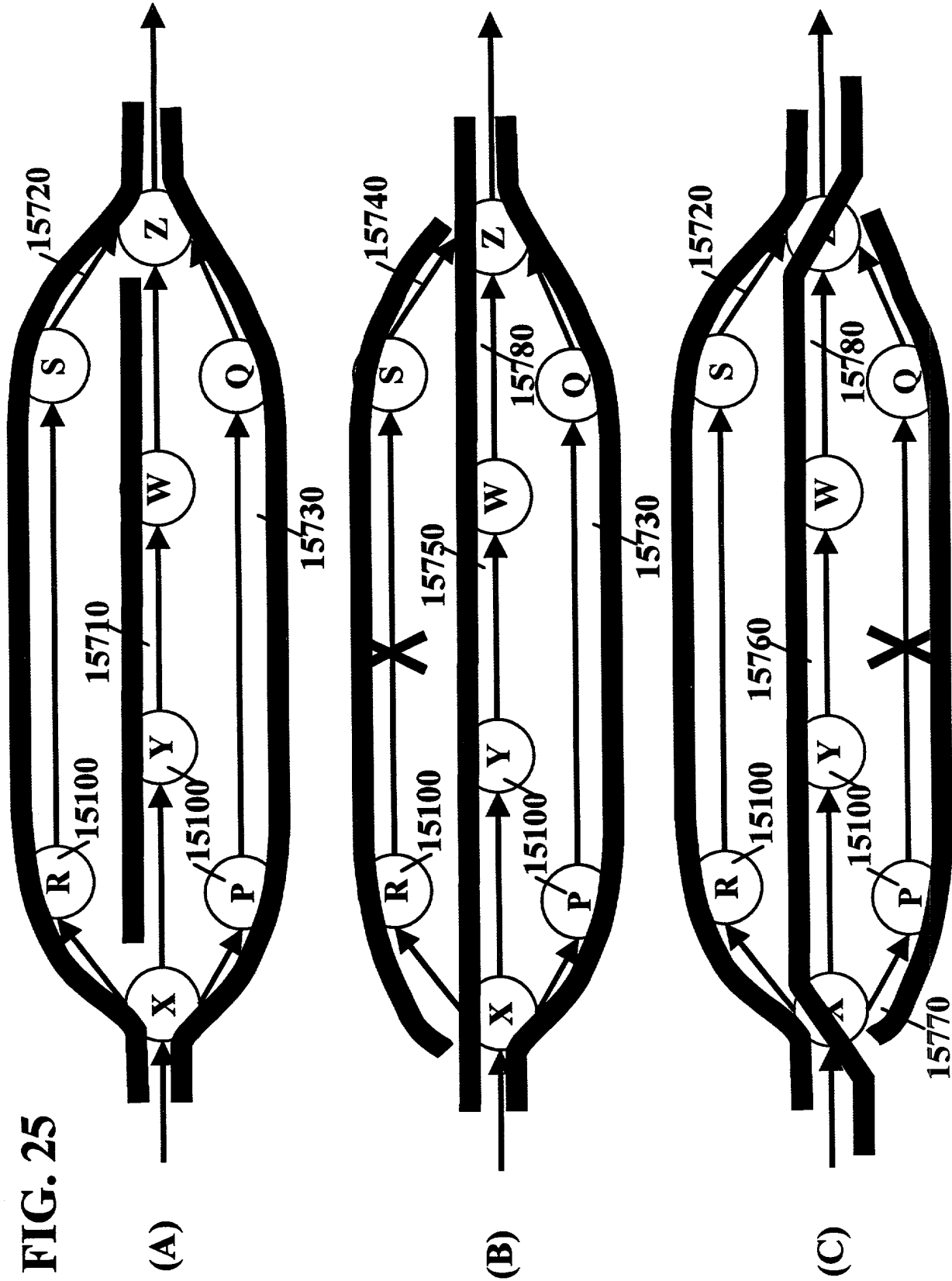


FIG. 25



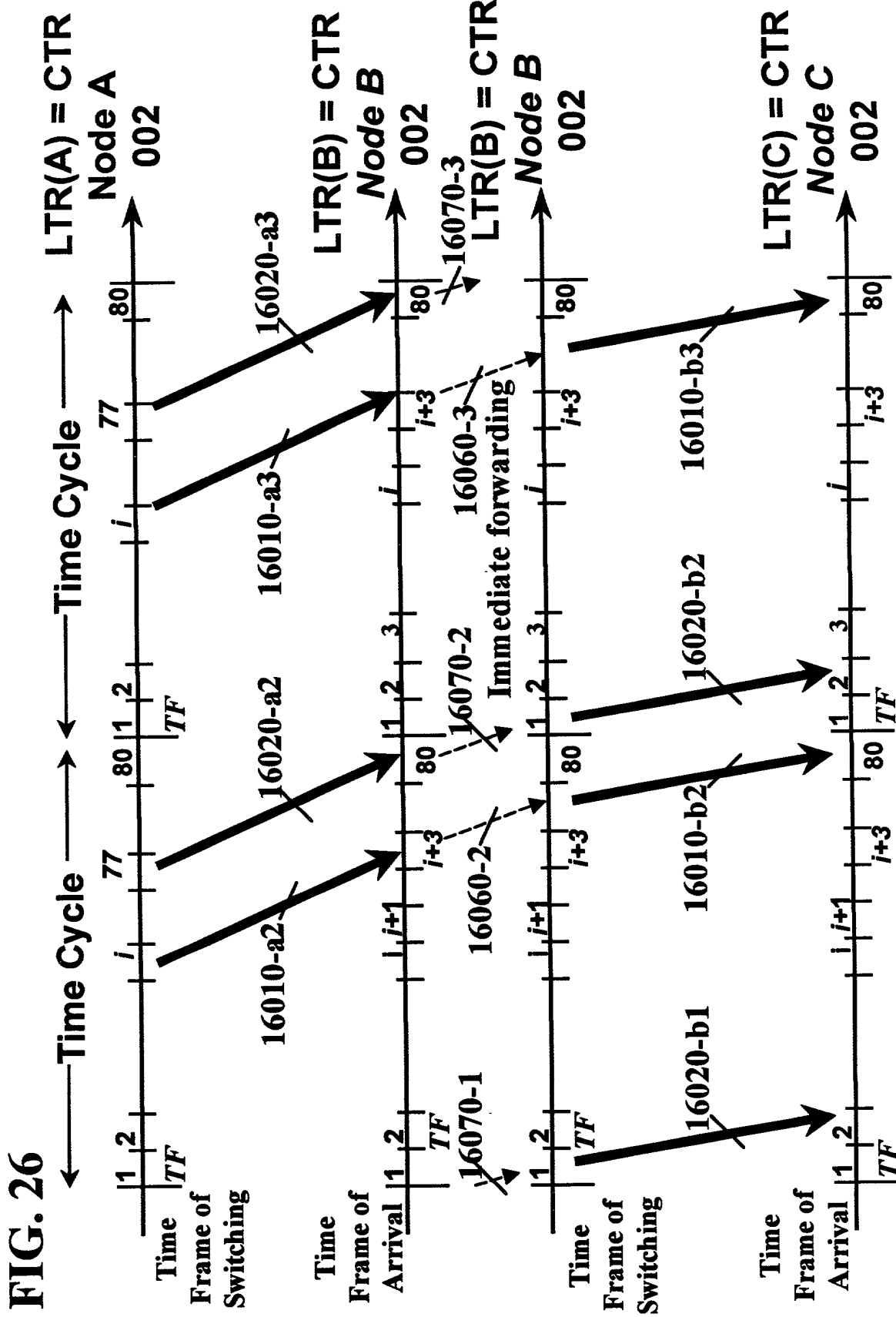
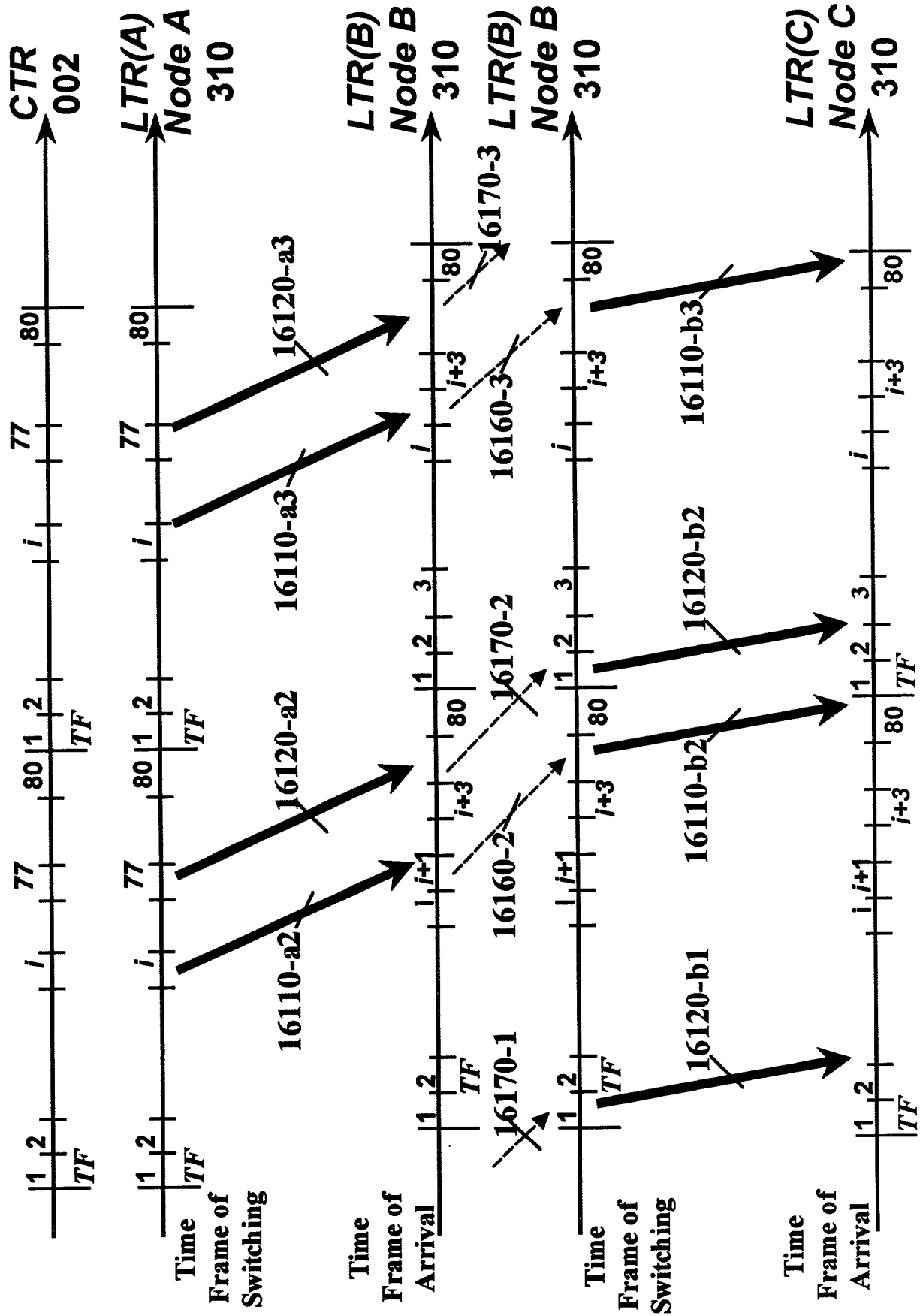
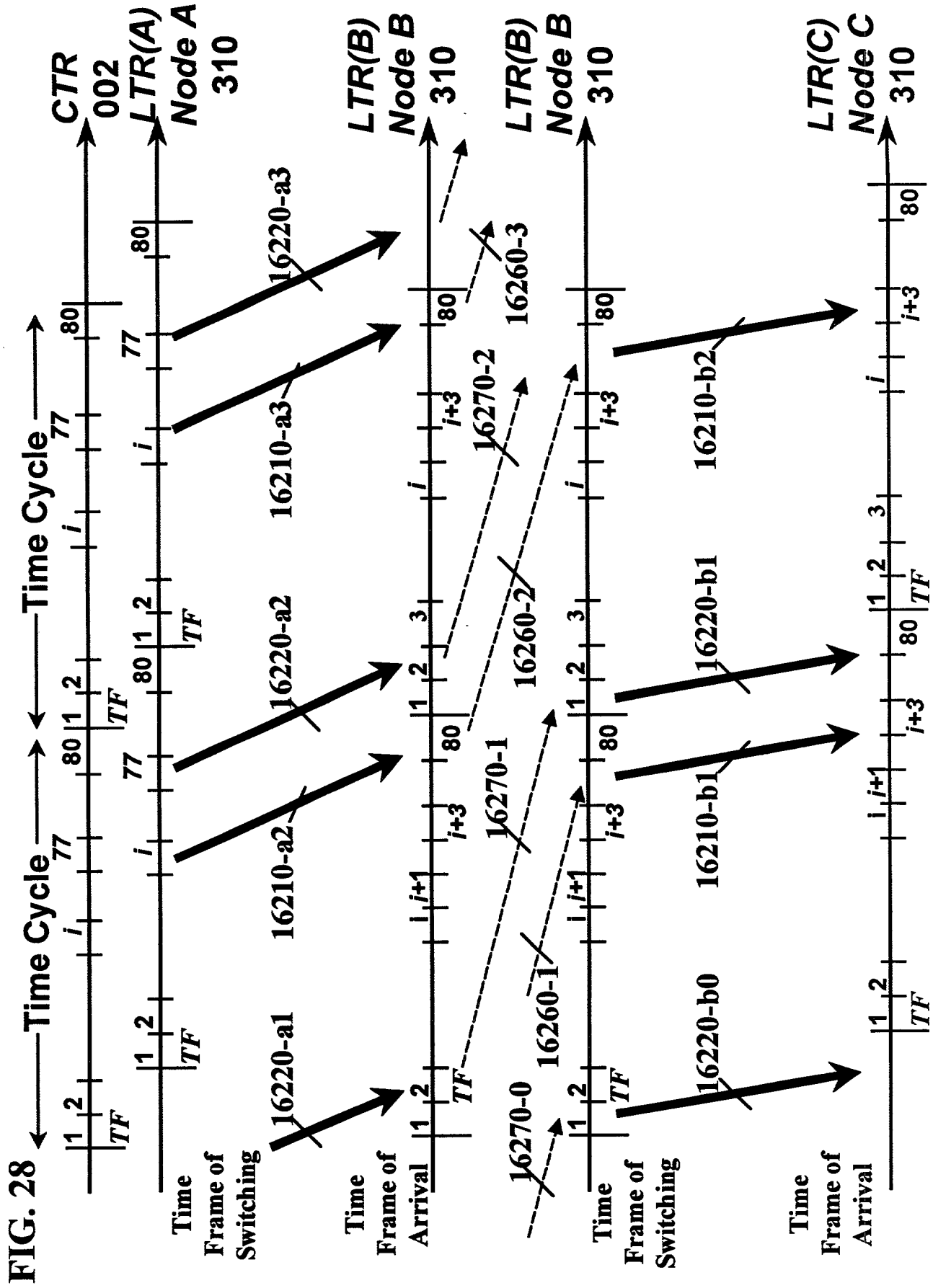


FIG. 27 ← Time Cycle → Time Cycle →





CTR-002

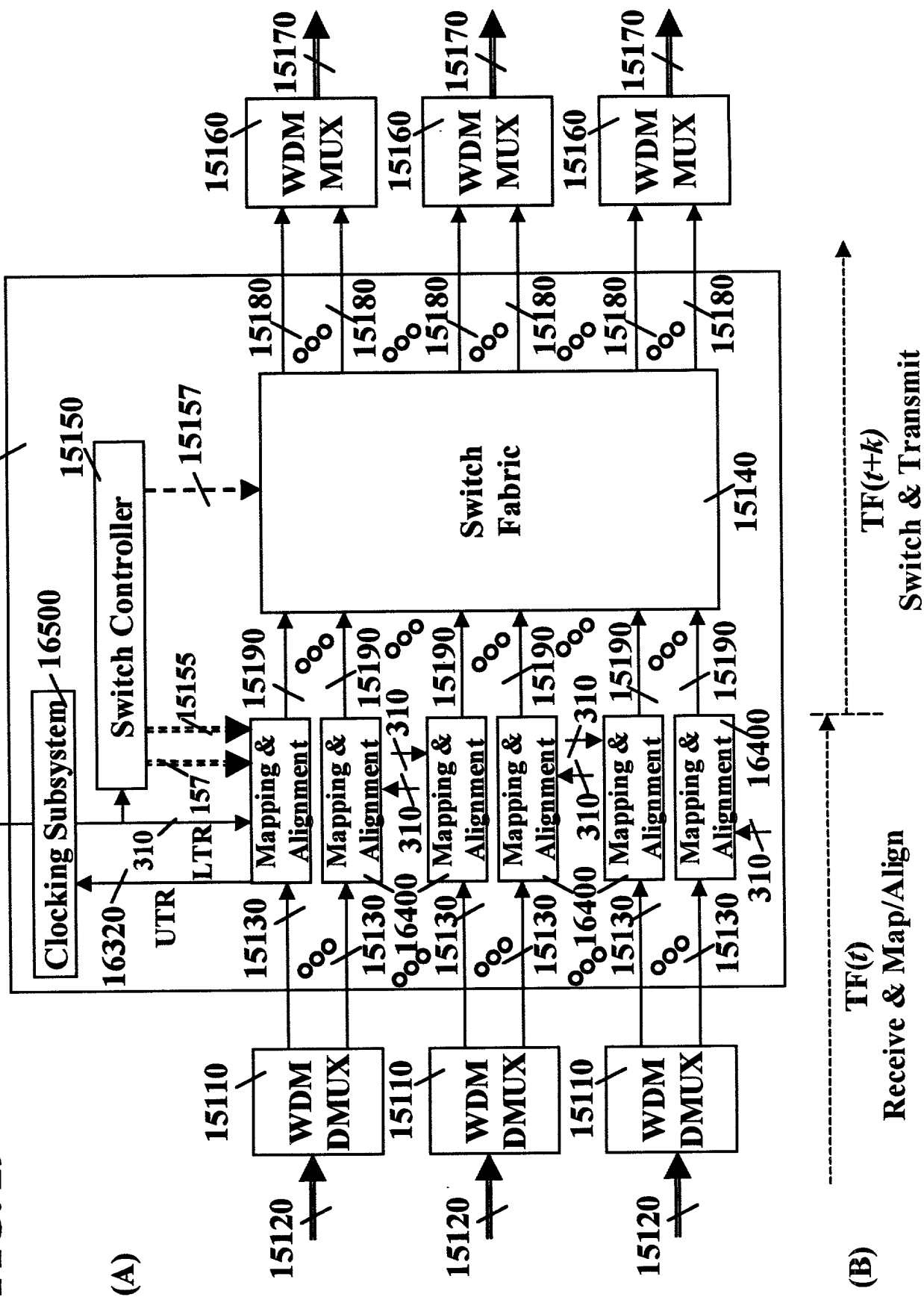


FIG. 30

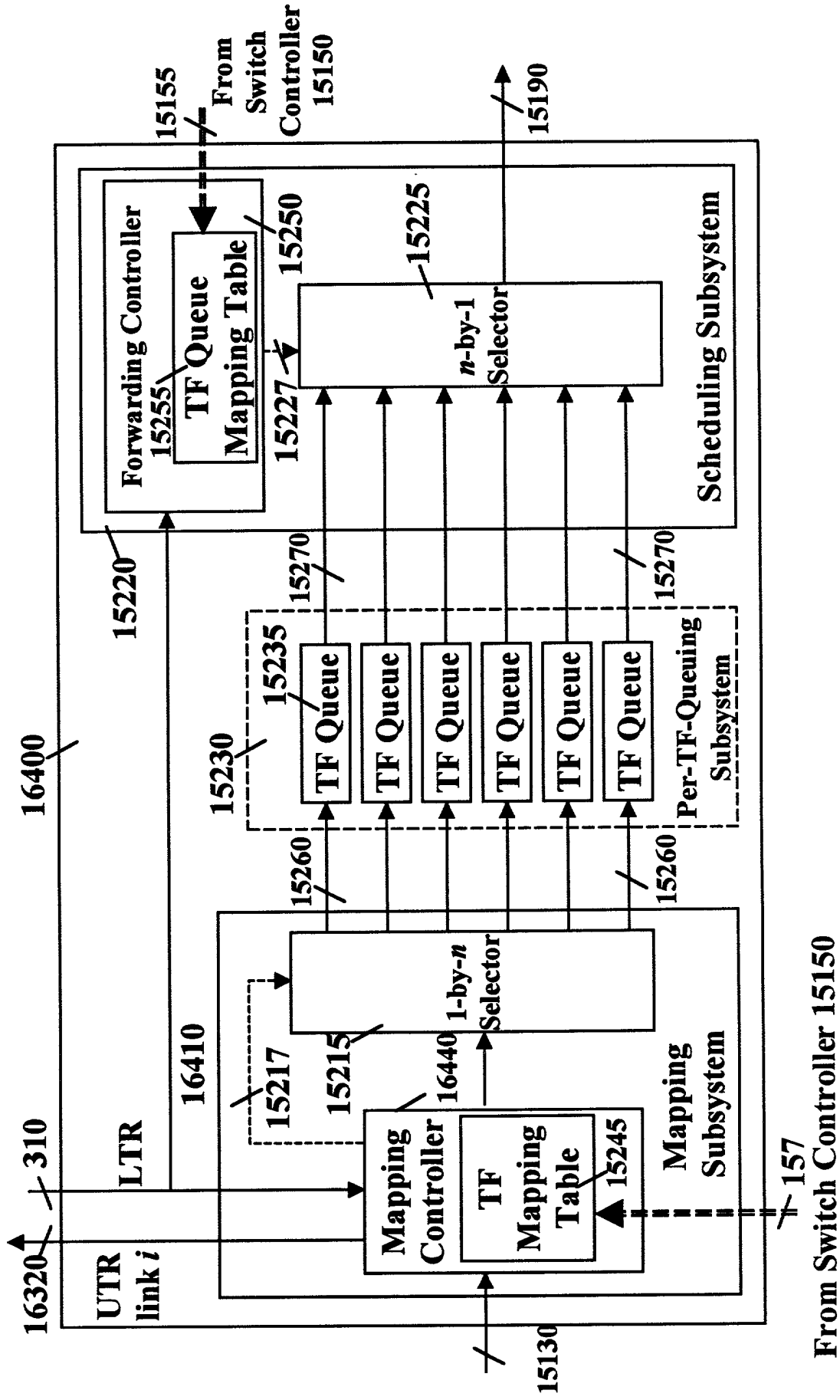


FIG. 31

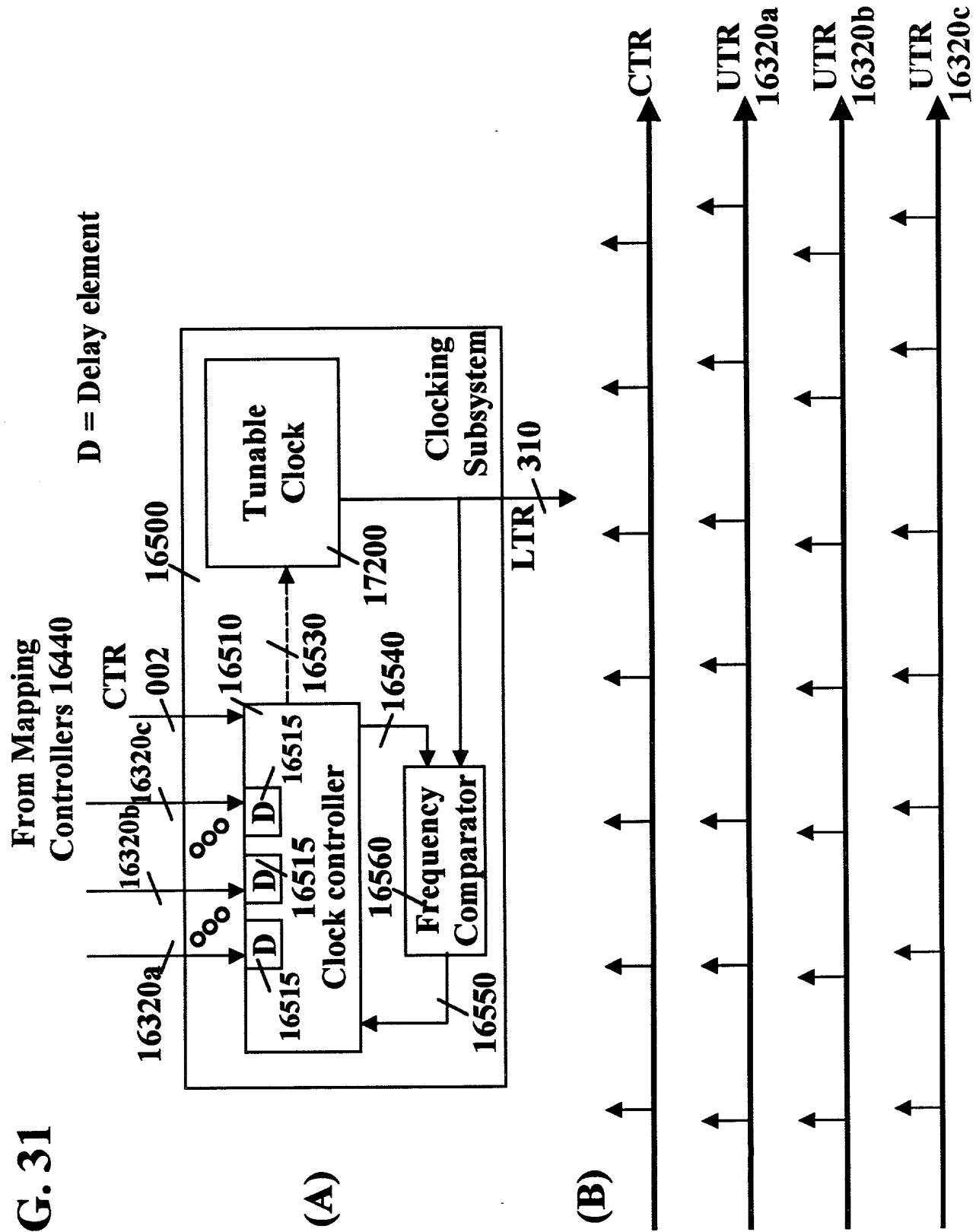


FIG. 32

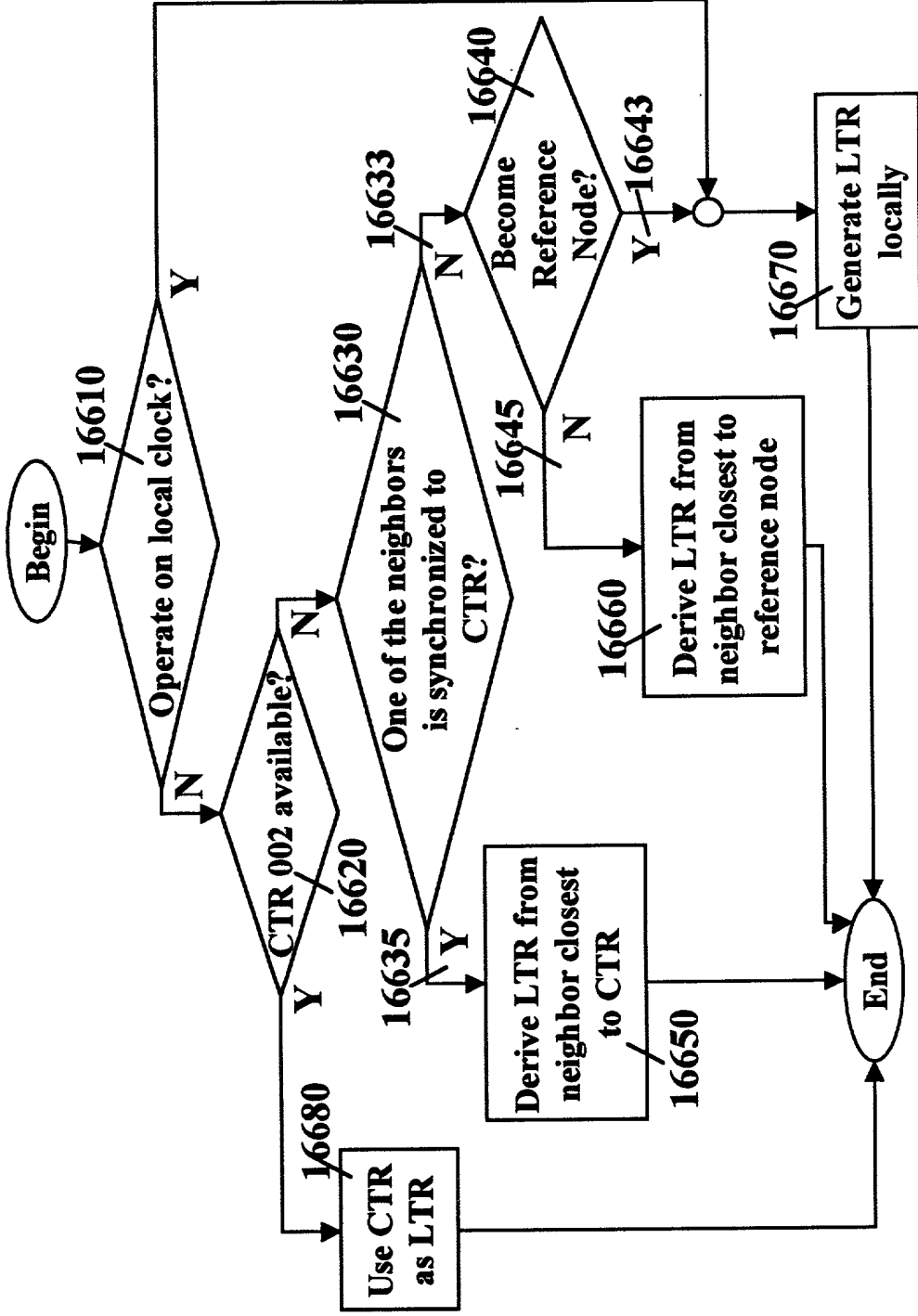


FIG. 33

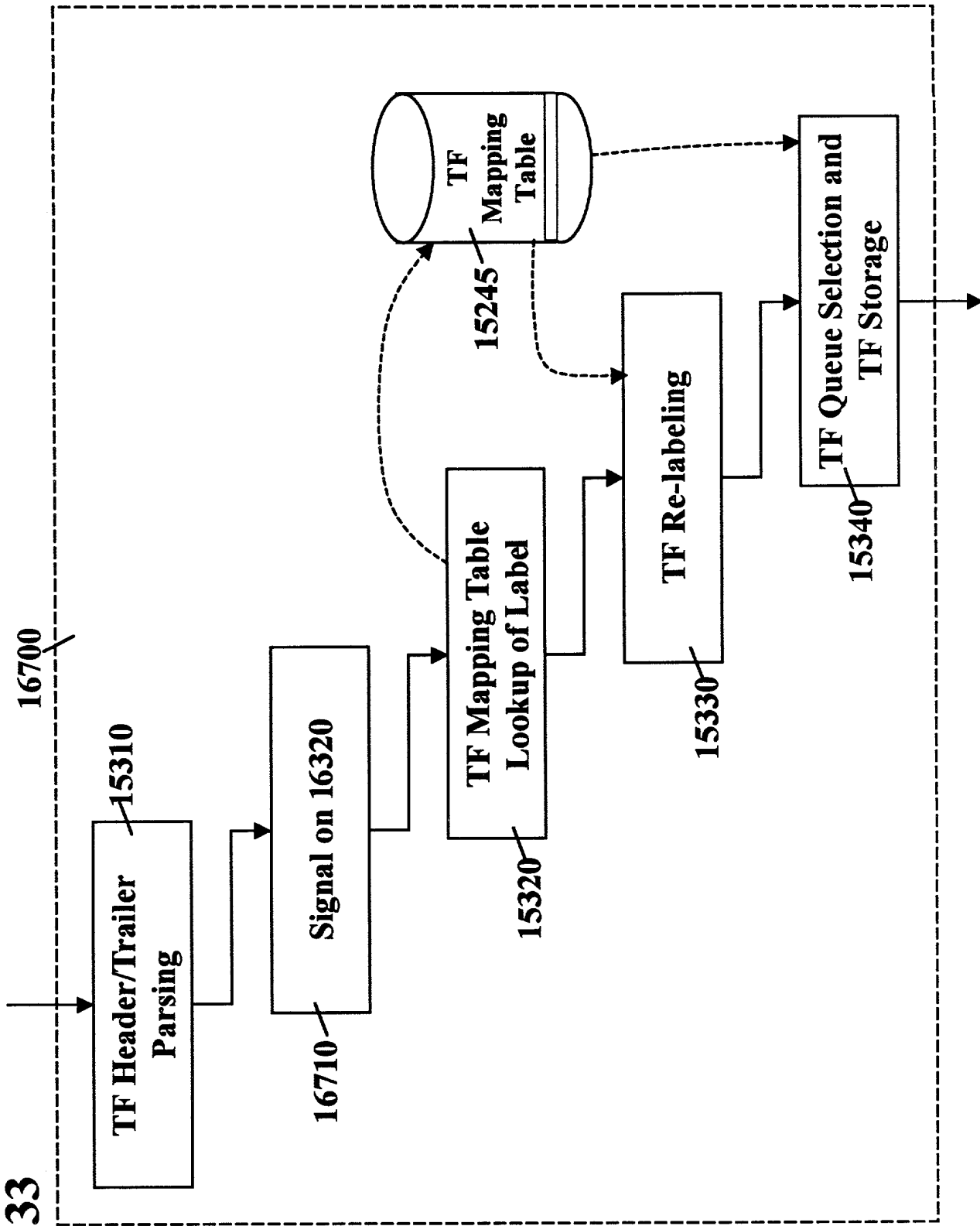
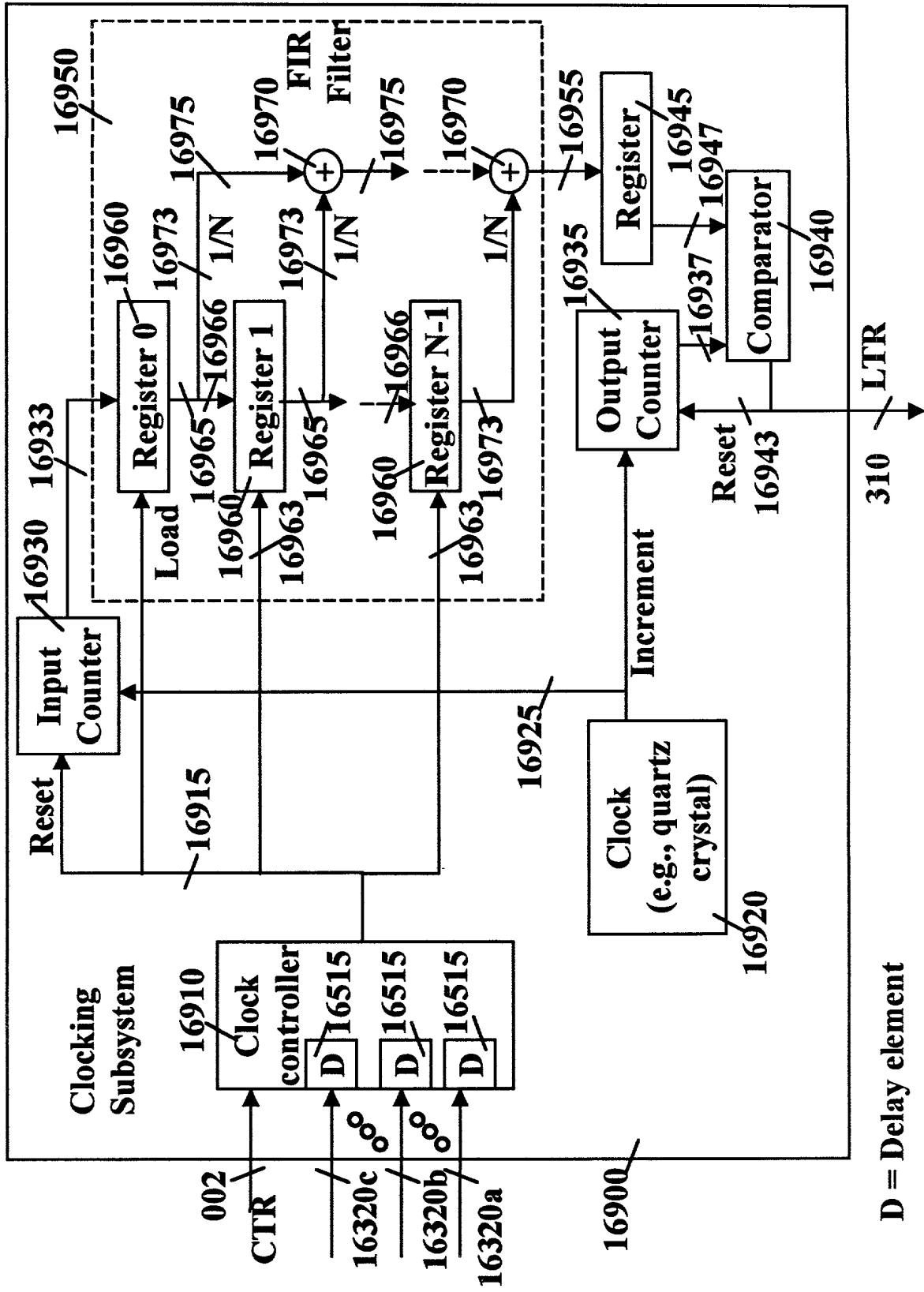


FIG. 34

TF duration [μs]	# TF queues	Memory req. [Kbytes]	Clock accuracy	Stratum	Tolerance				
					D	H	M	S	
7.8125	20	195	1.00E-10	1	7	16	27	42	
7.8125	20	195	1.60E-08	2	0	1	9	10	
7.8125	20	195	4.60E-06	3	0	0	0	14	
7.8125	20	195	3.20E-05	4	0	0	0	2	
7.8125	200	1,953	1.60E-08	2	0	13	21	35	
7.8125	200	1,953	4.60E-06	3	0	0	2	47	
7.8125	200	1,953	3.20E-05	4	0	0	0	24	
7.8125	1000	9,766	1.60E-08	2	2	19	36	48	
7.8125	1000	9,766	4.60E-06	3	0	0	14	6	
7.8125	1000	9,766	3.20E-05	4	0	0	2	1	
15.625	20	391	1.00E-10	1	15	8	55	25	
15.625	20	391	1.60E-08	2	0	2	18	20	
15.625	20	391	4.60E-06	3	0	0	0	28	
15.625	20	391	3.20E-05	4	0	0	0	4	
15.625	200	3,906	1.60E-08	2	1	2	43	11	
15.625	200	3,906	4.60E-06	3	0	0	5	34	
15.625	200	3,906	3.20E-05	4	0	0	0	48	
15.625	1000	19,531	1.60E-08	2	5	15	13	36	
15.625	1000	19,531	4.60E-06	3	0	0	28	13	
15.625	1000	19,531	3.20E-05	4	0	0	4	3	
31.25	20	195	1.00E-10	1	30	17	50	50	
31.25	20	195	1.60E-08	2	0	4	36	41	
31.25	20	195	4.60E-06	3	0	0	0	57	
31.25	20	195	3.20E-05	4	0	0	0	8	
31.25	200	1,953	1.60E-08	2	2	5	26	22	
31.25	200	1,953	4.60E-06	3	0	0	11	9	
31.25	200	1,953	3.20E-05	4	0	0	1	36	
31.25	1000	9,766	1.60E-08	2	11	6	27	12	
31.25	1000	9,766	4.60E-06	3	0	0	56	26	
31.25	1000	9,766	3.20E-05	4	0	0	8	6	

FIG. 35



D = Delay element

FIG. 36

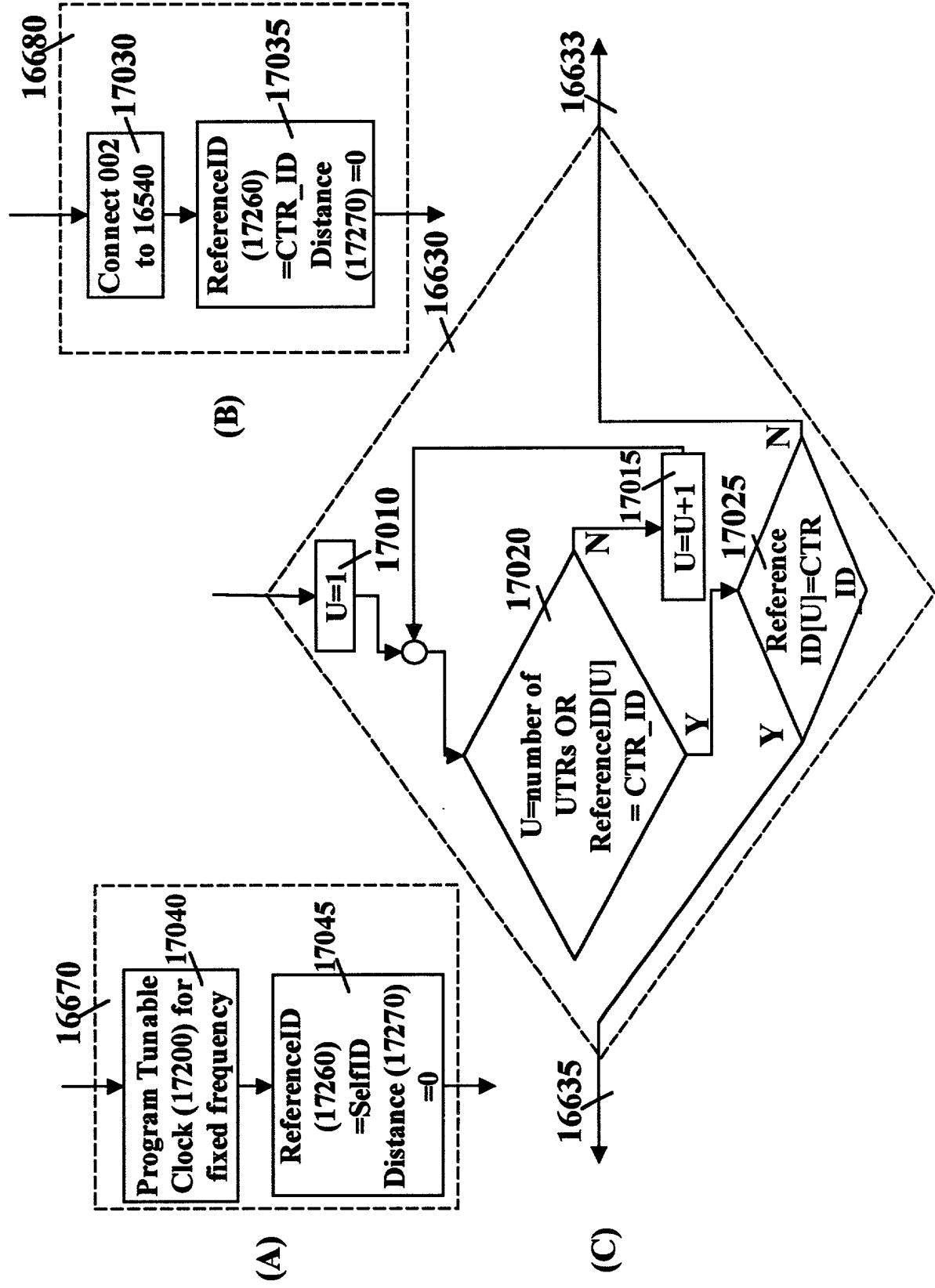


FIG. 37

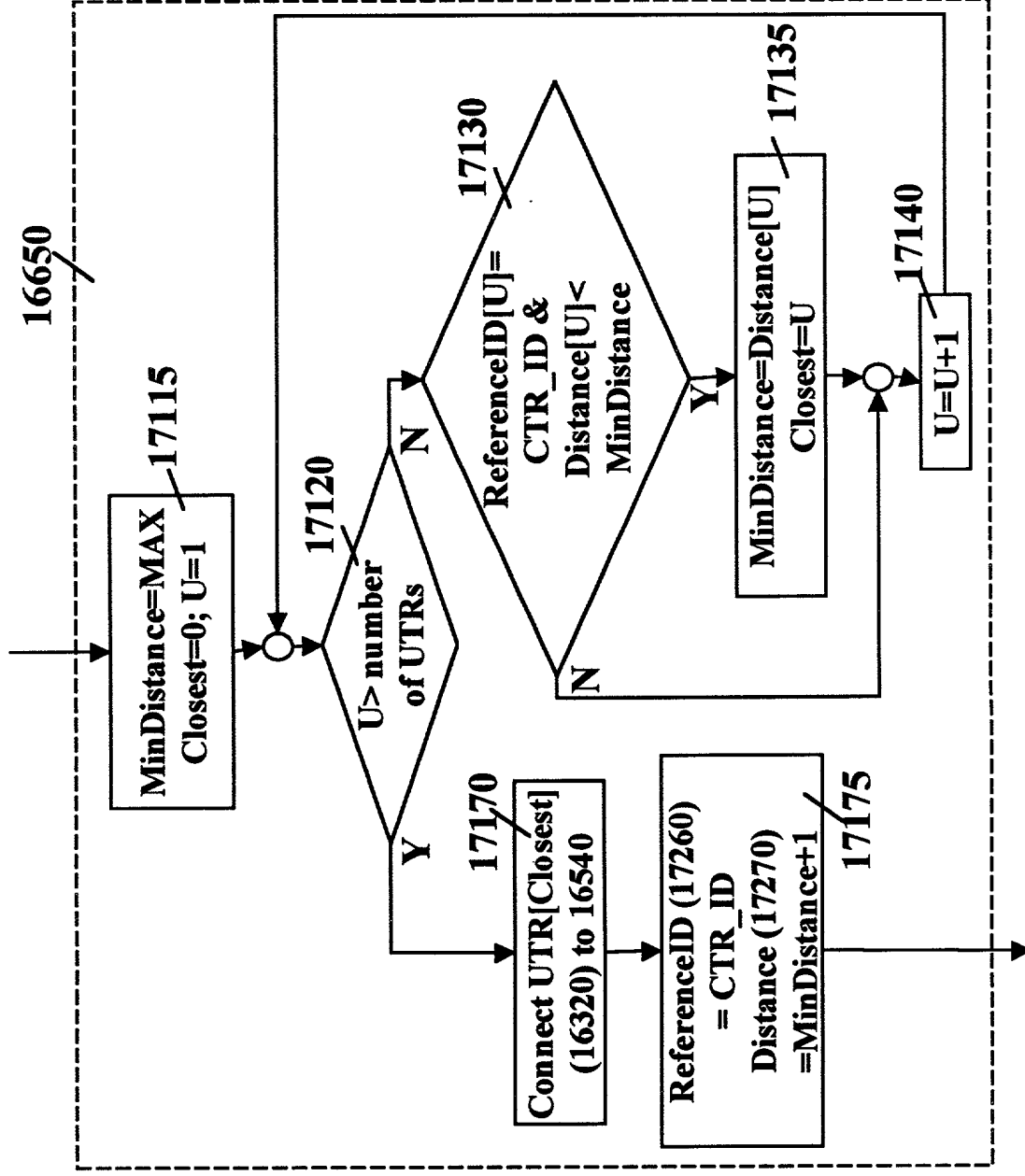
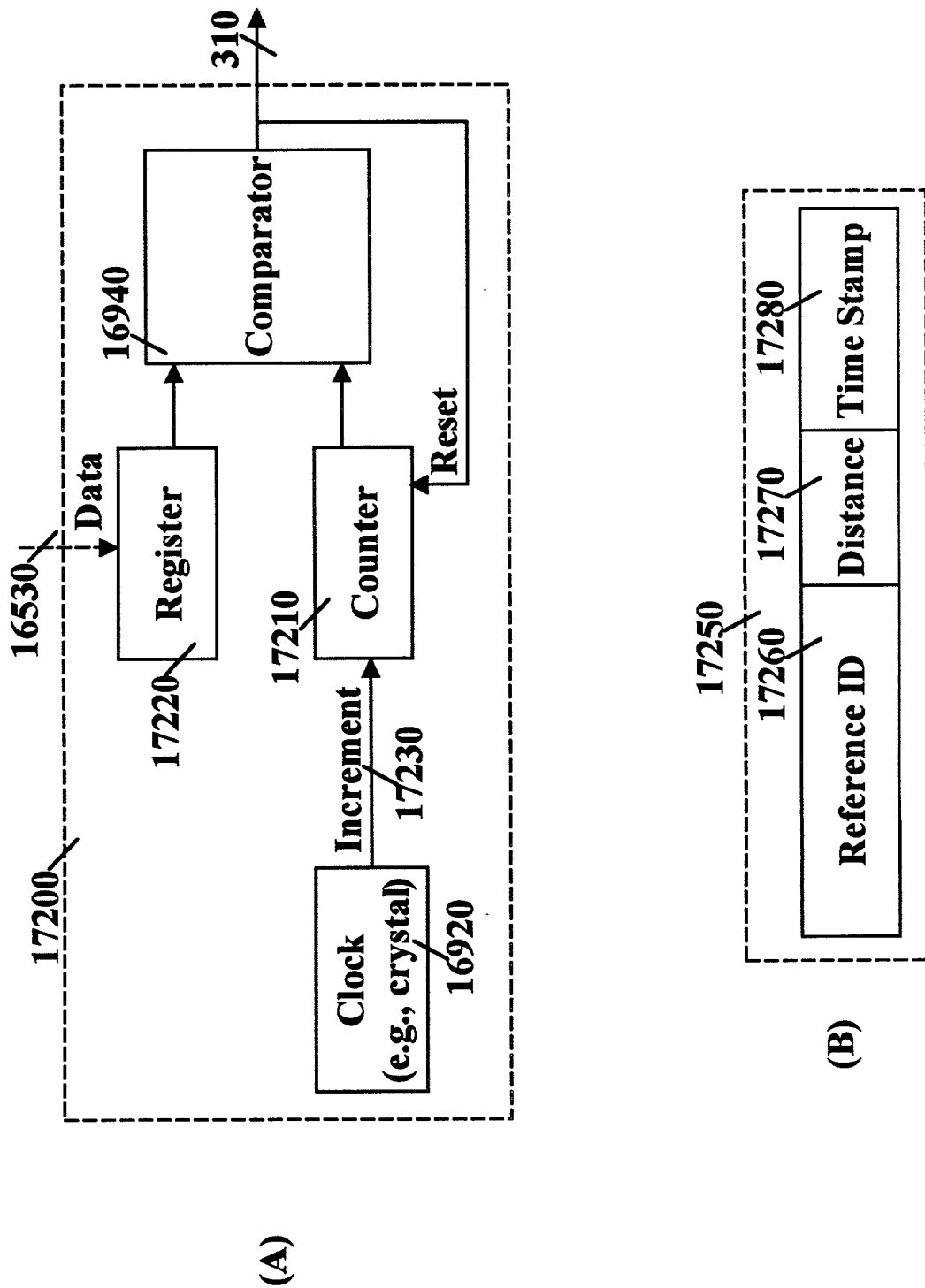


FIG. 38



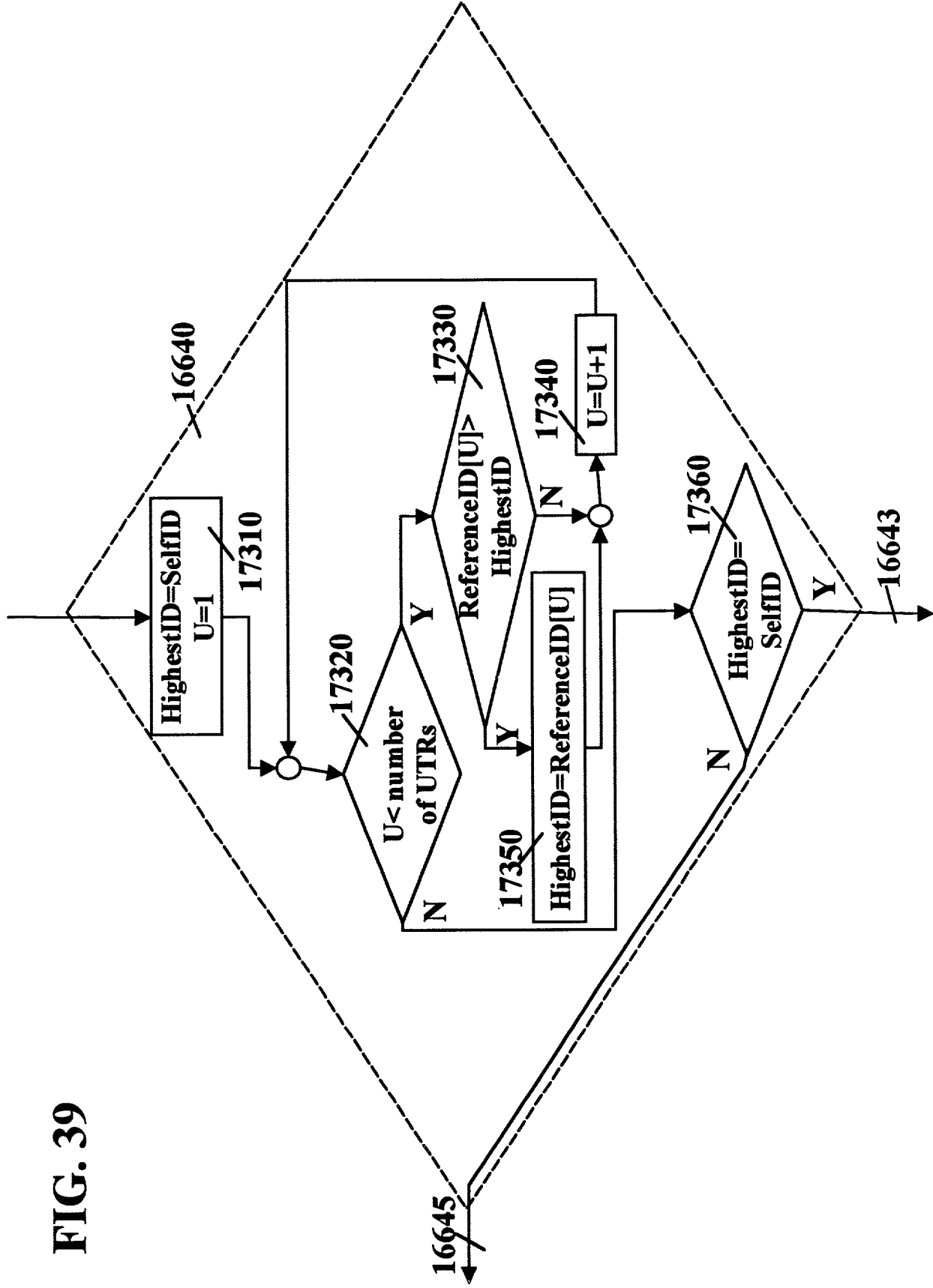


FIG. 39

FIG. 40

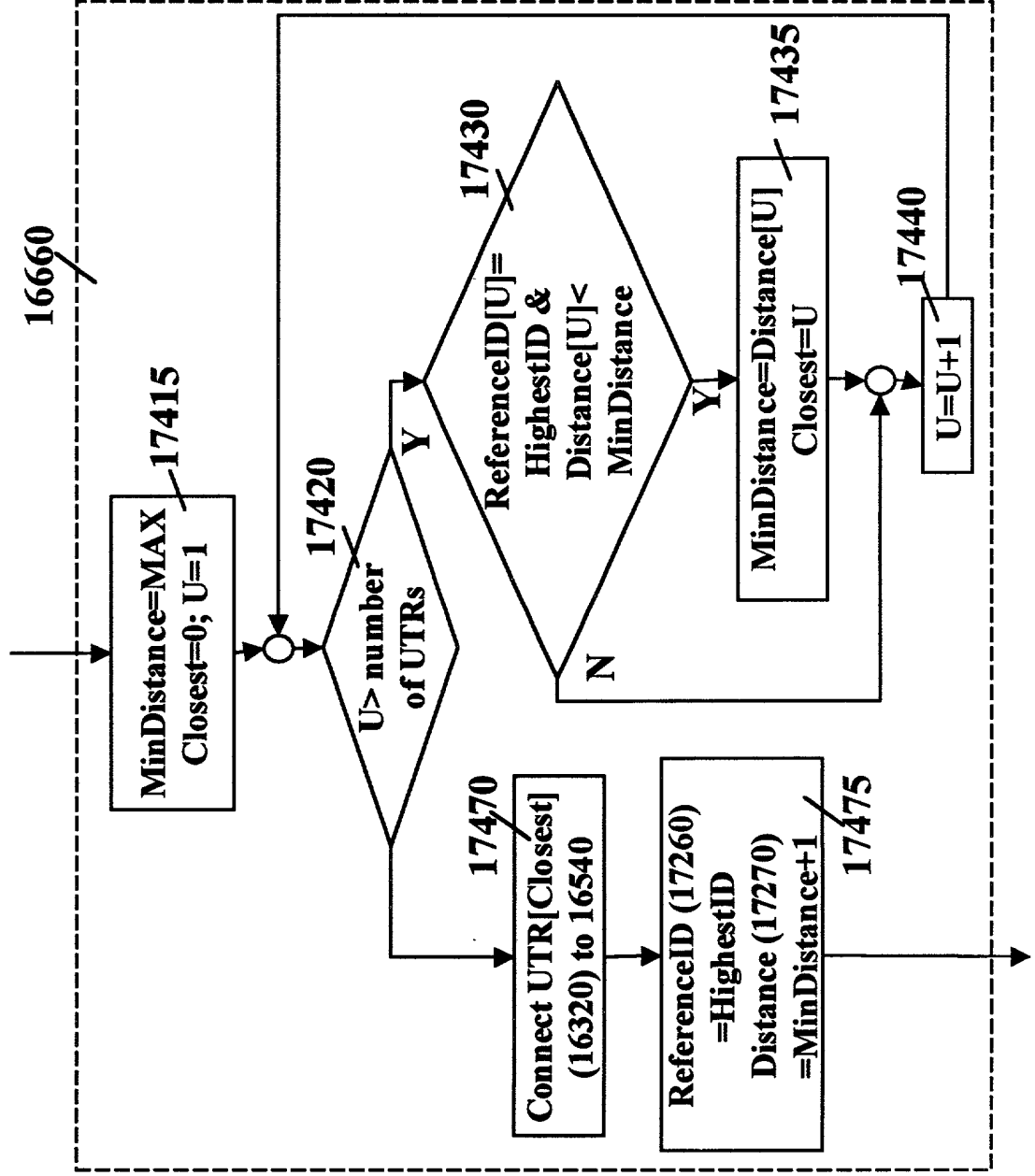


Figure 1 is a block diagram of a switch architecture. The diagram shows a central 'Switch Fabric' (4120) connected to multiple 'Input Subsystems' (4140u-1 to 4140u-N) and 'Output Subsystems' (4140a). Each subsystem includes an 'Alignment Subsystem' (4125) and a 'Switch Controller' (4110). The input subsystems receive 'Input 1' (4130) to 'Input N' (4130) and output 'Output 1' (4135) to 'Output N' (4135). The output subsystems output 'Output 1' (4135) to 'Output N' (4135). The diagram also shows a timeline with time slots (t-3, t-2, t-1, t, t+1, t+2) and a 'Time-of-Day or UTC' axis. A legend defines 'CTR' as Time frame, 'Tf' as Time frame payload, and '4140' as Time frame payload with a predefined number of data units.

4140 T_f : Time frame

Time frame payload – with a predefined number of data units

FIG. 42

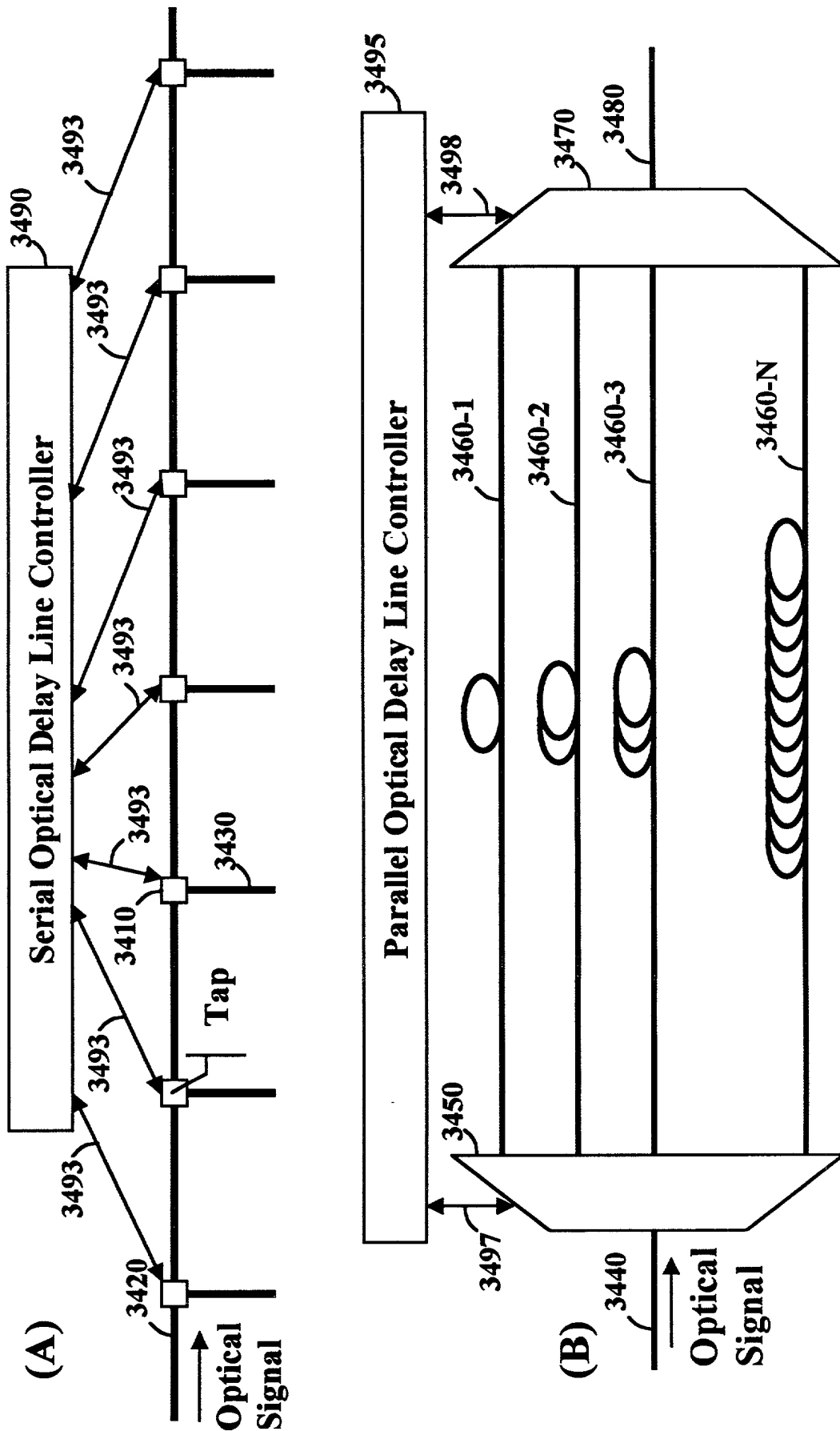
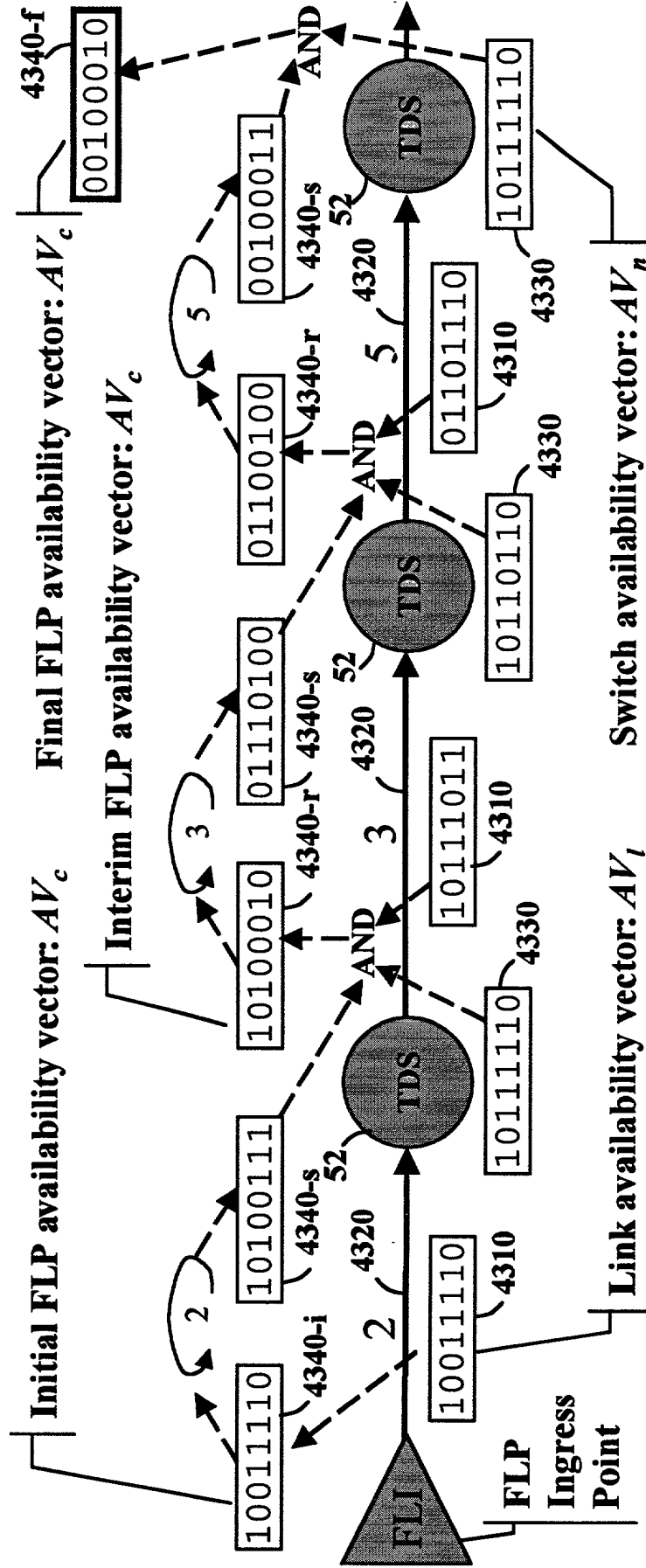


FIG. 43



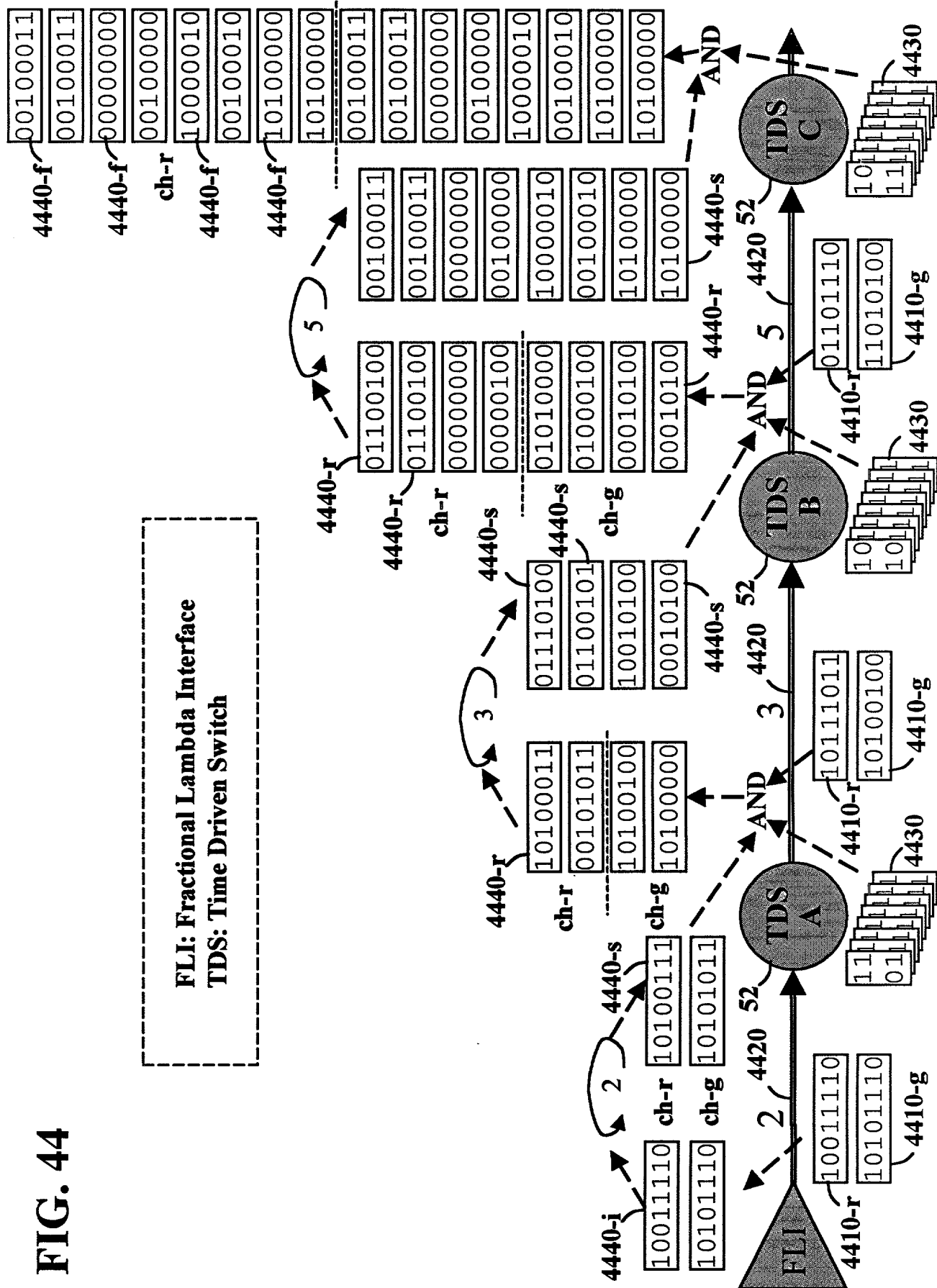


FIG. 44